DECchip 21052 PCI-to-PCI Bridge Evaluation Board

User's Guide

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Preface

This document describes the DECchip 21052 PCI-to-PCI Bridge Evaluation Board, which is an evaluation and development board for systems based on the DECchip 21052 PCI-to-PCI Bridge chip. The DECchip 21052 PCI-to-PCI Bridge Evaluation Board (also referred to as the EB52) complies with the electrical and protocol requirements of the *PCI Local Bus Specification, Revision 2.0* and the *PCI-to-PCI Bridge Architecture Specification, Revision 1.0*.

Audience

This document is for developers who are using the EB52 to design software for the DECchip 21052 PCI-to-PCI Bridge and to evaluate its functionality.

Content

This document contains the following chapters and an appendix:

- **Chapter 1, Introduction** — Describes the hardware and software requirements for using the EB52, and describes secondary slot numbering and IDSEL mapping, the jumpers on the EB52, and typical configurations.
- **Chapter 2, Interrupt Combining and Bus Arbitration** — Describes the interrupt combining and secondary bus arbitration functions.
- **Chapter 3, Kit Contents and Installation** — Lists the kit contents and provides the procedure for installing the EB52.
- **Appendix A, Technical Support, Ordering, and Associated Literature** — Provides information about ordering Digital's microprocessor and peripheral chips, and associated literature. It also explains how to obtain technical support and information.

Conventions

The following conventions are used in this guide:

Convention	Description
Notes	Provide additional information.
Signal names	Signals that connect to the DECchip 21052 PCI-to-PCI Bridge chip are defined as follows: • The leading letter indicates the source of the signal: – **s_** indicates the secondary PCI bus. – **p_** indicates the primary PCI bus. – **x** indicates that the signal is from the initiator or bus master. – **y** indicates that the signal is from the target or slave device. • The middle letters represent the signal name. • The **_l** suffix indicates that the signal is asserted low. Signals that are asserted high have no suffix. For example, **s_trdy_l** indicates that the secondary PCI bus signal **trdy** is asserted low.
Bits	The bit of the specified bused signal is indicated in angle brackets. For example, **s_ad<21>**. A pair of numbers in the angle brackets separated by a colon (:) indicates a multiple bit field. For example, **<7:3>** specifies bits 7, 6, 5, 4, and 3.

1 Introduction

This chapter describes the DECchip 21052 PCI-to-PCI Bridge chip and evaluation board (EB52). It describes the hardware and software requirements for using the board, secondary slot numbering and IDSEL mapping, how to configure the jumpers on the EB52, and typical configurations.

1.1 DECchip 21052 PCI-to-PCI Bridge

The DECchip 21052 PCI-to-PCI Bridge (also referred to as the 21052) is a low-cost, high-performance chip that enables multiple PCI buses in all PCI systems (Alpha, Pentium, X86, PowerPC). The 21052 allows motherboard designers to add more PCI devices or more PCI option-card slots than a single PCI bus can support. Option-card designers can use the 21052 to implement multiple device PCI option cards.

The 21052 has two PCI interfaces. The primary PCI interface connects directly to the PCI bus closest to the host CPU. The secondary PCI interface creates a new and independent PCI bus. The primary function of the bridge is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus.

The 21052 also allows the two PCI buses to operate independently. A master and a target located on the same PCI bus can communicate with each other even if the other PCI bus is busy. As a result, the 21052 can isolate traffic between devices on one PCI bus from devices on other PCI buses. This is a major benefit to system performance in some applications, such as multimedia.

For detailed information about the 21052, refer to the *DECchip 21052 PCI-to-PCI Bridge Data Sheet*.

1.2 DECchip 21052 PCI-to-PCI Bridge Evaluation Board

The DECchip 21052 PCI-to-PCI Bridge Evaluation Board (EB52) is a universal PCI expansion board that is used to evaluate the operation of the DECchip 21052 PCI-to-PCI Bridge in various configurations and with a variety of PCI devices. Using the EB52, you can

- Develop initialization code to configure a PCI-to-PCI bridge and the PCI devices behind the bridge.
- Evaluate the operation of the PCI-to-PCI bridge with a variety of PCI devices attached to the secondary bus.
- Build and evaluate a flexible hierarchy for multiple PCI buses.

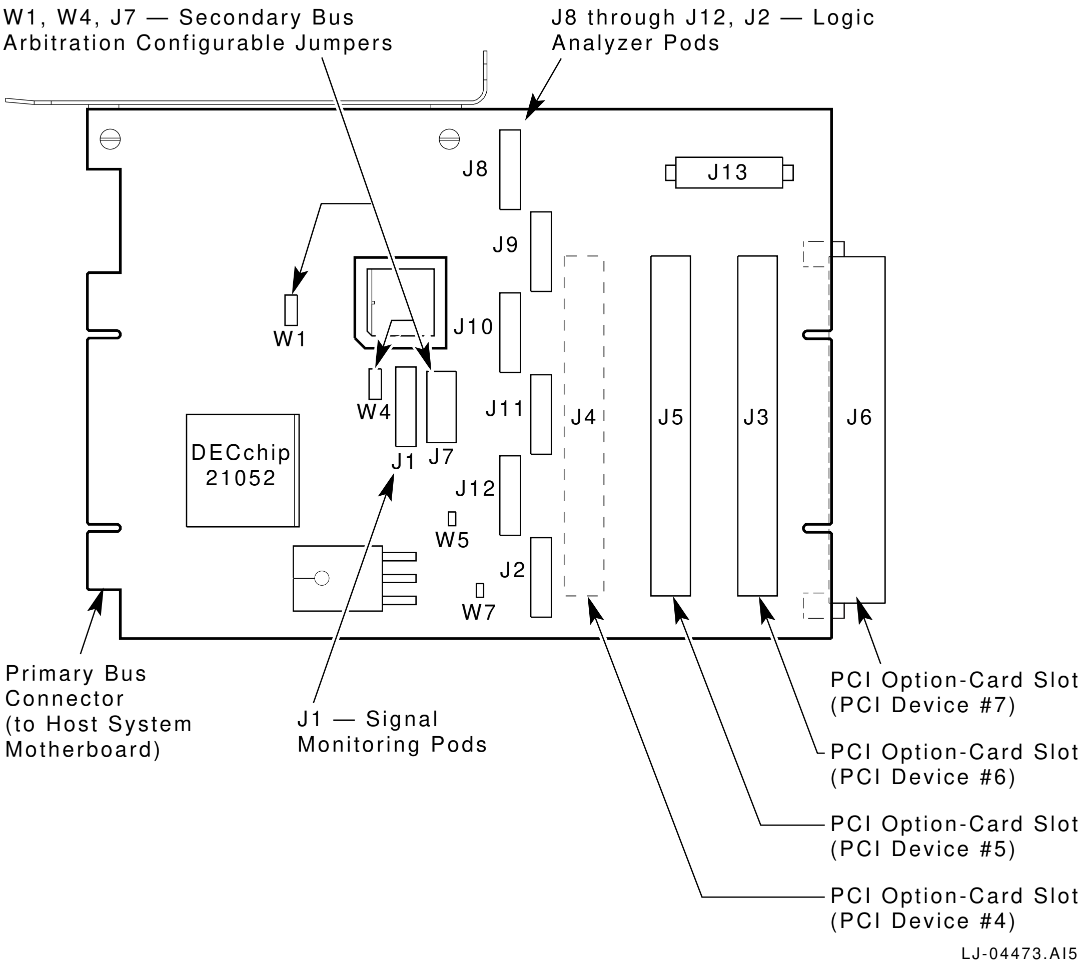
Figure 1–1 shows the major components on the EB52.

1.2.1 Features

The EB52 has the following features:

- A DECchip 21052 PCI-to-PCI bridge that provides bridging between a primary and secondary bus
- A primary PCI bus that plugs into any 5-volt or 3.3-volt PCI expansion-card slot
- Four secondary 5-volt PCI bus expansion-card slots
- Full protocol and electrical compliance to the *PCI Local Bus Specification, Revision 2.0*
- Selectable external secondary bus arbiter
- Support for multiple levels of PCI bus hierarchy

Figure 1–1 DECchip 21052 PCI-to-PCI Bridge Evaluation Board



1.2.2 Hardware Requirements

The following equipment is required to use the EB52:

- A computer system equipped with a PCI motherboard.
- Full compliance to the *PCI Local Bus Specification, Revision 2.0*.
- A PCI expansion slot equipped for the 5-volt or 3.3-volt environment.
- One or more PCI option-cards installed in the secondary expansion bus slots. If the secondary slots are empty, only bridge initialization is supported.

1.2.3 Software Requirements

To test the EB52 in X86 DOS or WINDOWS systems, system BIOS must include autoconfiguration code for PCI-to-PCI bridges. If the system BIOS does not include this functionality, contact your BIOS vendor to obtain code with PCI-to-PCI bridge autoconfiguration support.

The PCI-to-PCI bridge can be configured using the DOS utility provided with the EB52 kit. The README.TXT file on the shipped diskette provides information about using the DOS utility.

1.2.4 Specifications

The physical and power specifications for the EB52 are as follows:

Dimensions:

Height: 20.0 cm (7.90 in)

Width: 13.2 cm (5.20 in)

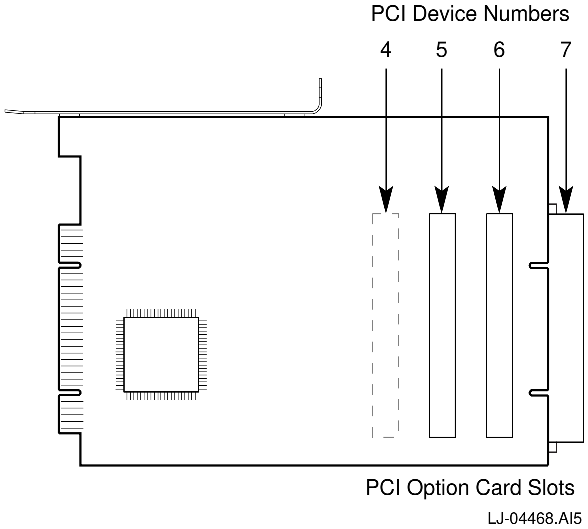
Power Requirements:

dc amps @ 5 volts: 2.0 A (maximum)

1.3 Secondary Slot Numbering and IDSEL Mapping

The PCI secondary bus expansion slots are mapped to device numbers 4, 5, 6, and 7 as shown in Figure 1–2. The secondary bus lines **s_ad<23:20>** are used as secondary IDSEL lines.

Figure 1–2 Secondary PCI Slot Numbering



1.4 Jumpers

There are ten jumpers on the EB52. Table 1–1 describes the jumpers, and Figure 1–1 shows their location.

Table 1–1 Jumpers on the EB52

Jumpers	Description
J1	Monitors the following signals: **clk_h** (PCI clock) **s_clk<1>** through **s_clk<4>** (four secondary PCI clocks) **s_clk** (**s_clk<0>** is fed back to the **s_clk** input pin)
W1, W4, J7	These are the secondary bus arbitration jumpers. Chapter 2 provides information about configuring these jumpers.
J2, J8 through J12	You can plug logic analyzer pods into these jumpers to monitor all secondary PCI signals of the bridge.

1.5 Typical Configurations

The EB52 supports various PCI configurations with different types of devices. Figures 1–3 through 1–6 are sample PCI configurations.

The primary bus connector attaches to a PCI slot on the motherboard of the host system or to a secondary PCI bus slot on another EB52. A 5-volt or universal option PCI card, or another EB52 can be plugged into any one of the four secondary bus option-card slots.

Figure 1–3 DECchip 21052 PCI-to-PCI Bridge Evaluation Board with One Secondary Bus Option-cards

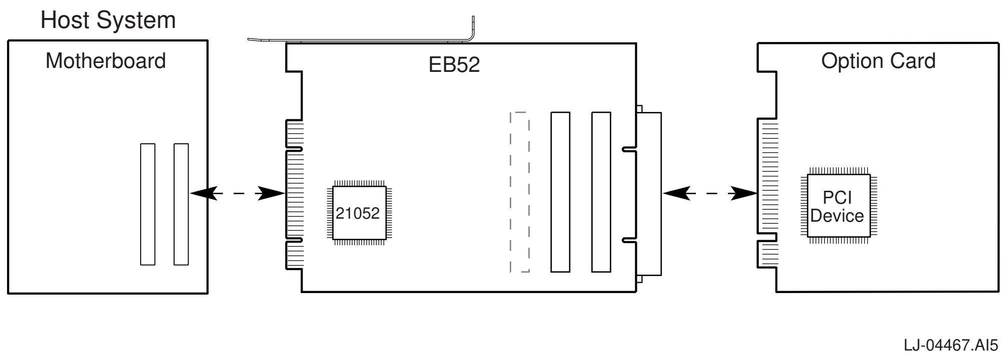


Figure 1–4 DECchip 21052 PCI-to-PCI Bridge Evaluation Board with Two Secondary Bus Option-cards

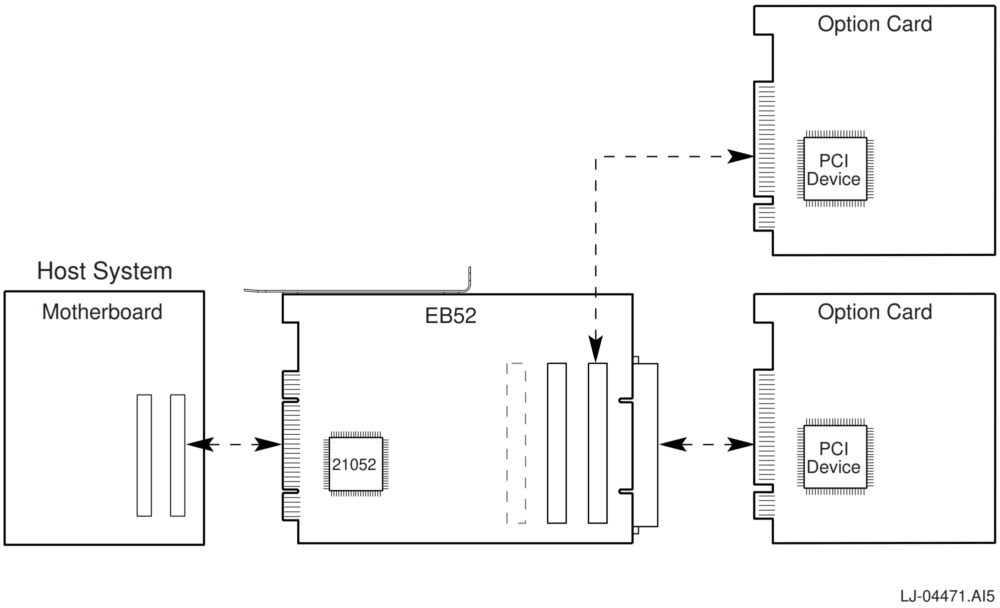


Figure 1–5 Tri-Level Bus with Two DECchip 21052 PCI-to-PCI Bridge Evaluation Boards

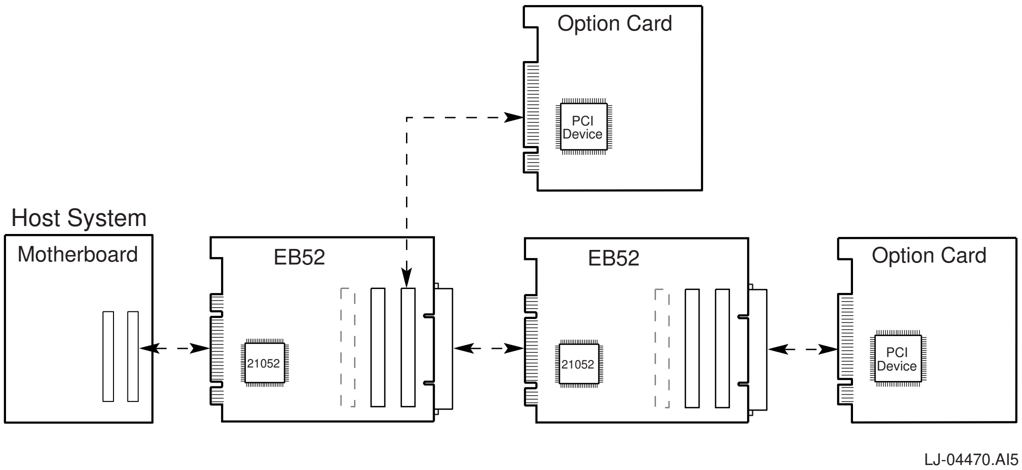
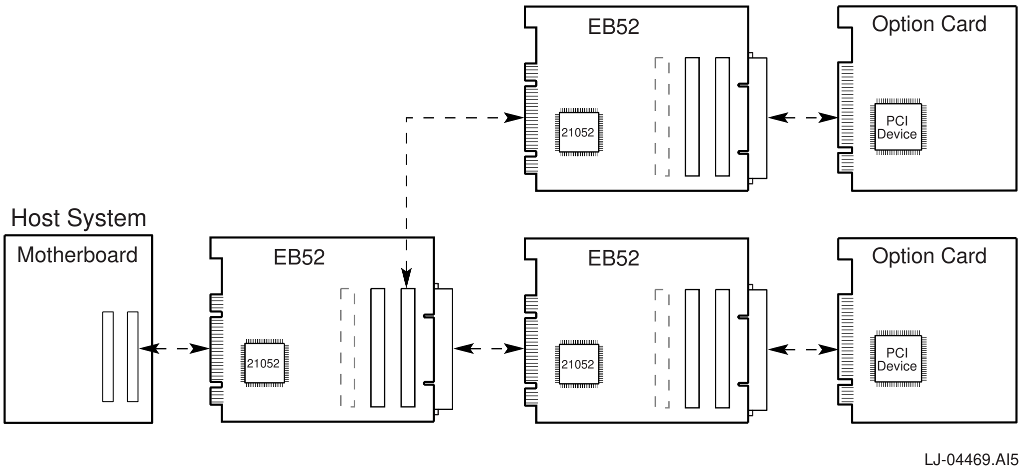


Figure 1–6 Four PCI Buses in a 3-Level Hierarchy



2 Interrupt Combining and Bus Arbitration

This chapter describes the interrupt combining and secondary bus arbitration functions.

2.1 Interrupt Combining

Because a total of 16 interrupts are connected to the secondary bus PCI slots (INTA#, INTB#, INTC#, and INTD# for each slot) and only four interrupts are driven to the card edge, the 16 incoming interrupts must be combined. This ORing of interrupts is performed in accordance with the *PCI-to-PCI Bridge Architecture Specification*.

Table 2–1 shows the ORing of interrupts.

Table 2–1 Interrupt ORing

Device Number	Interrupt Pin on Device	Interrupt Pin on Board Connector
4	INTA#	INTA#
	INTB#	INTB#
	INTC#	INTC#
	INTD#	INTD#
5	INTA#	INTB#
	INTB#	INTC#
	INTC#	INTD#
	INTD#	INTA#
6	INTA#	INTC#
	INTB#	INTD#
	INTC#	INTA#
	INTD#	INTB#
7	INTA#	INTD#
	INTB#	INTA#
	INTC#	INTB#
	INTD#	INTC#

In accordance with the *PCI Bridge Architecture Specification, Revision 1.0*, interrupts of the devices on the secondary slots are wire ORed and routed to PCI fingers of the EB52. Table 2–2 lists the interrupts from the devices on the secondary slots to the interrupts on the EB52 fingers.

Note

In the first column of Table 2–2, the number after each interrupt pin is the device number from the devices in the secondary slots. The L indicates that the assertion level is low.

Table 2–2 Interrupts from Devices to EB52 Fingers

Interrupts from Devices on Secondary Slots	Interrupts on EB52 Fingers
INTA4 L INTD5 L INTC6 L INTB7 L	INTA L
INTB4 L INTA5 L INTD6 L INTC7 L	INTB L
INTC4 L INTB5 L INTA6 L INTD7 L	INTC L
INTD4 L INTC5 L INTB6 L INTA7 L	INTD L

2.2 Secondary Bus Arbitration

The EB52 has two secondary bus arbiter systems — an internal arbiter implemented in the 21052 and an external arbiter implemented in an AMD MACH210A programmable device. The internal 21052 arbiter can be configured to operate in rotating or modified rotating mode. In modified rotating mode, the bridge is given highest priority on alternate transactions. Secondary bus parking is done by default at the 21052.

The external arbiter system resides in the PAL and implements straight-rotating arbitration. Secondary bus parking is done at the 21052. If a different external arbiter is used where parking is done at one of the PCI slots, a PCI device must be installed in that slot.

The default setting is internal arbitration. To change the default, refer to the jumper information in the next section.

2.2.1 Bus Arbitration Jumpers

To configure the secondary bus arbiter system, use jumpers J7, W4, and W1. All jumper positions assume that the EB52 is positioned with the components facing forward and the card edge facing down. See Figure 2–1 for the jumper locations. Tables 2–3 and 2–4 describe the jumper positions.

Figure 2–1 Jumper Locations

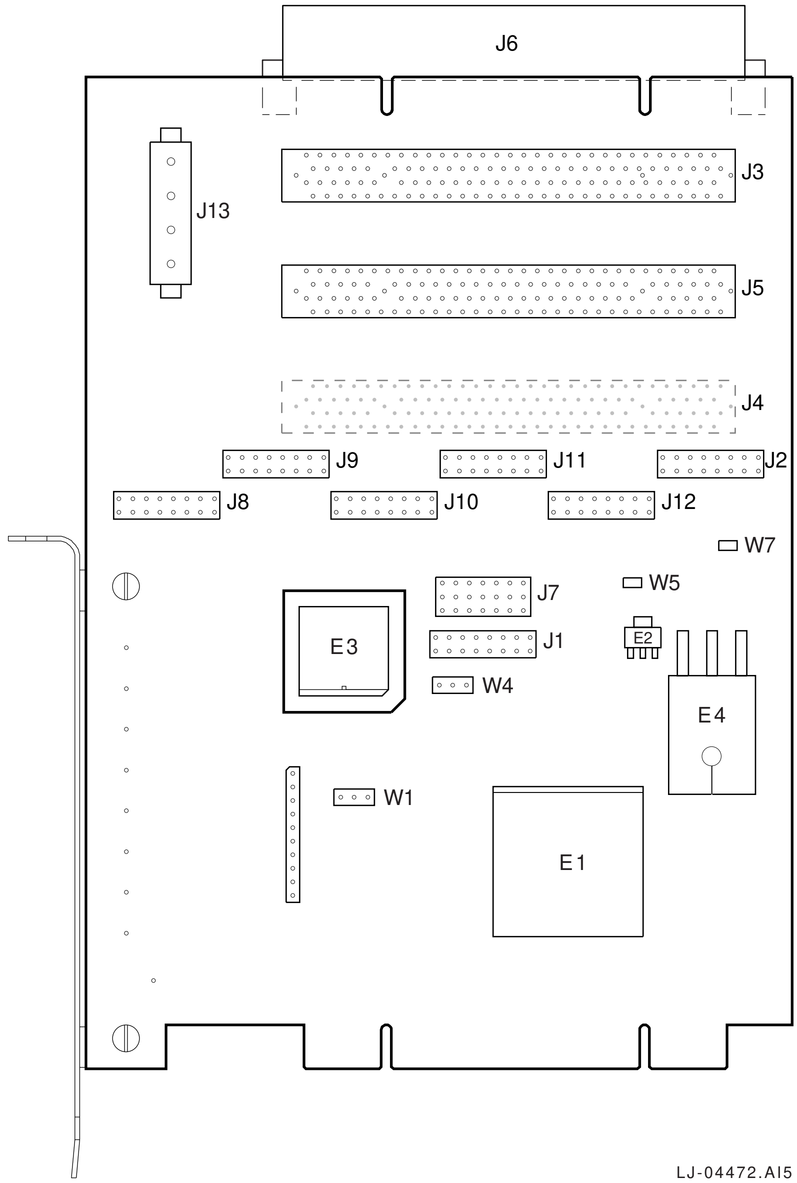


Table 2–3 Internal 21052 Arbitration

Jumper	Position	Description
J7	Bottom	Selects the 21052 as the source of secondary grant signals.
W4	Left	Selects the board signal **s_req_l<0>** (device 4 request signal) to drive the bridge **s_req_l<0>** input.
W1	Left	Ties **s_cfn_l** low, which enables the 21052 internal arbiter. When the secondary PCI bus is idle, parking is at the 21052.

Table 2–4 External PAL Arbitration

Jumper	Position	Description
J7	Top	Selects the PAL as the source of secondary grants.
W4	Right	Selects the board signals **gt_out<3>** (the external secondary grant to the 21052) to drive the bridge **s_req_l<0>** input.
W1	Right	Ties **s_cfn_l** high, which disables the internal 21052 arbiter and causes the following reconfigurations: • **s_gnt_l<0>** becomes the secondary bus request. • **s_req_l<0>** becomes the secondary bus grant. The PAL parks the secondary bus at the 21052.

3

Kit Contents and Installation

This chapter lists the contents of the DECchip 21052 PCI-to-PCI Bridge Evaluation Board Kit and describes how to install the DECchip 21052 PCI-to-PCI Bridge Evaluation Board.

3.1 Kit Contents

The DECchip 21052 PCI-to-PCI Bridge Evaluation Board Kit contains the following materials:

- DECchip 21052 PCI-to-PCI Bridge Evaluation Board (EB52)
- A diskette that contains a DOS utility for configuring the EB52
- A documentation package that includes the following:
  - *DECchip 21052 PCI-to-PCI Bridge Data Sheet*
  - *DECchip 21052 PCI-to-PCI Bridge Product Brief*
  - *DECchip 21052 PCI-to-PCI Bridge Configuration: An Application Note*
  - *DECchip 21052 PCI-to-PCI Bridge Hardware Implementation: An Application Note*
  - *DECchip 21052 Evaluation system BIOS Letter*
  - *DECchip 21052 Evaluation Board Vendor Parts List*
  - *DECchip 21052 PCI Evaluation Board Schematics*
  - Warranty agreement/registration card

3.2 Installation Procedure

To install the EB52, do the following:

1. Power down the PCI slot on the motherboard of the host system that will contain the EB52.
2. Place the motherboard with the associated support devices on a bench. This is necessary because mechanical constraints may not allow testing of the EB52 and the expansion slots inside the system box.
3. Insert the card edge of the EB52 into the powered down PCI slot.
4. Plug a 5-volt or universal option PCI card, or another EB52 into any one or more of the four secondary bus option-card slots. The Typical Configurations section in Chapter 1 shows sample PCI configurations.
5. Power on the PCI slot containing the EB52.
6. Test autoconfiguration and device operation as follows:
   a. Make sure the system BIOS or firmware detects and configures the PCI devices downstream of the 21052. If system BIOS is not available, use the DOS utility provided with the EB52 kit to configure the devices downstream of the 21052.
   b. Install the device driver for the PCI devices downstream of the 21052, and make sure that the device operates correctly.
7. If desired, monitor the secondary PCI signals of the bridge by connecting a logic analyzer to pods J2 and J8 through J12.

A

Technical Support, Ordering, and Associated Literature

This appendix provides information about ordering Digital's microprocessor and peripheral chips, and associated literature. It also explains how to obtain technical support and information.

A.1 Digital Semiconductor Information Line

Use the following numbers to call the Digital Semiconductor Information Line for information and technical support:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

A.2 Ordering Digital Semiconductor Products

To order the following Digital Semiconductor products, contact your local Digital sales office or local distributor.

Product	Order Number
DECchip 21052 PCI-to-PCI Bridge	21052–AA

A.3 Ordering Associated Literature

The following table lists DECchip 21052 literature that is available. For ordering information, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21052 PCI-to-PCI Bridge Product Brief	EC–QHUQA–TE
DECchip 21052 PCI-to-PCI Bridge Data Sheet	EC–QHURA–TE
DECchip 21052 PCI-to-PCI Bridge Configuration: An Application Note	EC–QLZBA–TE
DECchip 21052 PCI-to-PCI Bridge Hardware Implementation: An Application Note	EC–QLZAA–TE

A.4 Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor.

Title	Vendor
PCI Local Bus Specification, Revision 2.0 PCI-to-PCI Bridge Architecture Specification, Revision 1.0	PCI Special Interest Group M/S HF3–15A 5200 N.E. Elam Young Pkwy Hillsboro, Oregon 97124–6497 (503) 696–2000