AlphaServer 8200/8400 System Technical Manual Supplement: Memory

Order Number: EK–MS7CC–TS. A01

This document is a supplement to the *AlphaServer 8200/ 8400 System Technical Manual*. It discusses the specific features of the 4-Gbyte MS7CC-GA memory module. A maximum of seven MS7CC-GA memory modules can be configured in a system, offering a total memory capacity of 28 gigabytes.

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Contents

Figures

Tables

Preface

Intended Audience

This manual describes the MS7CC-GA 4-gigabyte memory module designed for use in AlphaServer 8200 and 8400 systems. It provides an overview of the operations of the memory module and gives detailed information on the subsystem registers. The manual is intended for technical professionals such as operating system programmers and customer service engineers.

Document Structure

This manual has three chapters:

- **Chapter 1, Introduction,** gives an overview of the MS7CC-GA memory module.
- **Chapter 2, Registers,** describes in detail the TLSB required and memory-specific registers.
- **Chapter 3, Self-Test,** gives a general discussion of the self-test of the MS7CC-GA memory module.

Documentation Titles

Table 1 lists the books in the DIGITAL AlphaServer 8200 and 8400 documentation set. Table 2 lists other documents that you may find useful.

Table 1 DIGITAL AlphaServer 8200 and 8400 Documentation

Title	Order Number
Hardware User Information and Installation	
Operations Manual	EK–T8030–OP
Site Preparation Guide	EK–T8030–SP
AlphaServer 8200 Installation Guide	EK–T8230–IN
AlphaServer 8400 Installation Guide	EK–T8430–IN
Service Information Kit	QZ–00RAC–GC
Service Manual (hard copy)	EK–T8030–SV
Service Manual (diskettes)	AK–QKNFA–CA AK–QUW7A–CA AK–QUW6A–CA
Reference Manuals	
System Technical Manual	EK–T8030–TM
System Technical Manual Supplement: CPU	EK–T8030–TS
System Technical Manual Supplement: Memory	EK–MS7CC–TS
DWLPA/DWLPB PCI Adapter Technical Manual	EK–DWLPX–TM
Upgrade Manuals for Both Systems	
KN7CC CPU Installation Card	EK–KN7CC–IN
KN7CD CPU Installation Card	EK–KN7CD–IN
KN7CE CPU Installation Card	EK–KN7CE–IN
MS7CC Memory Installation Card	EK–MS7CC–IN
KFTHA System I/O Module Installation Card	EK–KFTHA–IN
KFTIA Integrated I/O Module Installation Card	EK–KFTIA–IN

Table 1 DIGITAL AlphaServer 8200 and 8400 Documentation (Continued)

Title	Order Number
Upgrade Manuals: 8400 System Only	
AlphaServer 8400 Upgrade Manual	EK–T8430–UI
BA654 DSSI Disk PIU Installation Guide	EK–BA654–IN
BA655 SCSI Disk and Tape PIU Installation Guide	EK–BA655–IN
DWLAA Futurebus+ PIU Installation Guide	EK–DWLAA–IN
DWLMA XMI PIU Installation Guide	EK–DWLMA–IN
DWLPA/DWLPB PCI PIU Installation Guide	EK–DWL84–IN
H7237 Battery PIU Installation Guide	EK–H7237–IN
H7263 Power Regulator Installation Card	EK–H7263–IN
KFMSB Adapter Installation Guide	EK–KFMSB–IN
KZMSA Adapter Installation Guide	EK–KXMSX–IN
RRDCD Installation Guide	EK–RRDRX–IN
Upgrade Manuals: 8200 System Only	
DWLPA/DWLPB PCI Shelf Installation Guide	EK–DWL82–IN
H7266 Power Regulator Installation Card	EK–H7266–IN
H7267 Battery Backup Installation Card	EK–H7267–IN

Table 2 Related Documents

Title	Order Number
General Site Preparation	
Site Environmental Preparation Guide	EK–CSEPG–MA
System I/O Options	
BA350 Modular Storage Shelf Subsystem Configuration Guide	EK–BA350–CG
BA350 Modular Storage Shelf Subsystem User's Guide	EK–BA350–UG
BA350-LA Modular Storage Shelf User's Guide	EK–350LA–UG
CIXCD Interface User Guide	EK–CIXCD–UG
DEC FDDIcontroller 400 Installation/Problem Solving	EK–DEMFA–IP
DEC FDDIcontroller/Futurebus+ Installation Guide	EK–DEFAA–IN
DEC FDDIcontroller/PCI User Information	EK–DEFPA–IN
DEC LANcontroller 400 Installation Guide	EK–DEMNA–IN
DSSI VAXcluster Installation/Troubleshooting Manual	EK–410AA–MG
EtherWORKS Turbo PCI User Information	EK–DE435–OM
KZPSA PCI-to-SCSI Storage Adapter User's Guide	EK–KZPSA–UG
RF Series Integrated Storage Element User Guide	EK–RF72D–UG
StorageWorks RAID Array 200 Subsystem Family Installation and Configuration Guide	EK–SWRA2–IG
Architecture Reference Manual	
Alpha Architecture Reference Manual	EY–L520E–DP
MEMORY CHANNEL Manuals	
MEMORY CHANNEL User's Guide	EK–PCIRM–UG
MEMORY CHANNEL Service Information	EK–PCIRM–SV

Chapter 1

Introduction

The MS7CC-GA is a single-capacity memory module that provides 4 gigabytes of dynamic random access memory (DRAM) to the CPU. A subsystem can be configured on an AlphaServer 8400 with a maximum of seven MS7CC-GA modules providing a total memory capacity of 28 Gbytes.

1.1 Features

The MS7CC-GA memory modules feature the following:

- 4 Gbytes of memory capacity divided across four separate banks. Each bank is 1 Gbyte in size.
- 1 Gbit SIMM based on 16-Mbit deep x 4-bit wide DRAM components
- Incremental configuration to a maximum of seven modules implemented on extended-hex +1" size boards in a dual-processor AlphaServer 8400 system
- Up to 16-way interleaving of memory banks
- 64-byte block transfers, executed in two 32-byte transfers over two contiguous data cycles
- Read and write data wrapping on 32-byte naturally aligned boundaries
- Quadword ECC protection that allows single-bit error detection and correction, and double-bit error detection.

The MS7CC-GA modules can coexist in the same system with all other TLSB compatible memory modules. They run synchronously with the TLSB, so that no additional synchronization logic or clocks are required.

Memory modules are responders only. Memory transactions are initiated by commanders (CPUs or I/O nodes) on the command/address bus. Memory data transfers are initiated over a separate 256-bit data bus. All transactions on the data bus are retired in the order in which they were received on the command/address bus.

TLSB systems can support a maximum of 16 memory banks. Seven MS7CC-GA memory modules, however, may have up to 28 separate memory banks. This would make it impossible to build a maximally configured memory system with MS7CC-GA memory modules.

This architectural constraint is resolved with the implementation of a configuration mode that allows two memory banks to be configured as one bank. In this configuration mode, each MS7CC-GA has two memory banks, 2 gigabytes per bank. This mode allows one the maximum configuration of seven memory modules (16 memory banks, with one module having four banks) to be installed on a single TLSB.

During memory writes, TLSB memory modules store write data and ECC check bits as they are received off the TLSB. A minor modification of the ECC check bits is done before they are written to the DRAMs to allow for the addition of a row parity bit and a column parity bit to provide additional data integrity protection. During memory reads, memory modules strip off the encoded Row/Col parity bits from the ECC check bits prior to asserting the read data and check bits onto the TLSB.

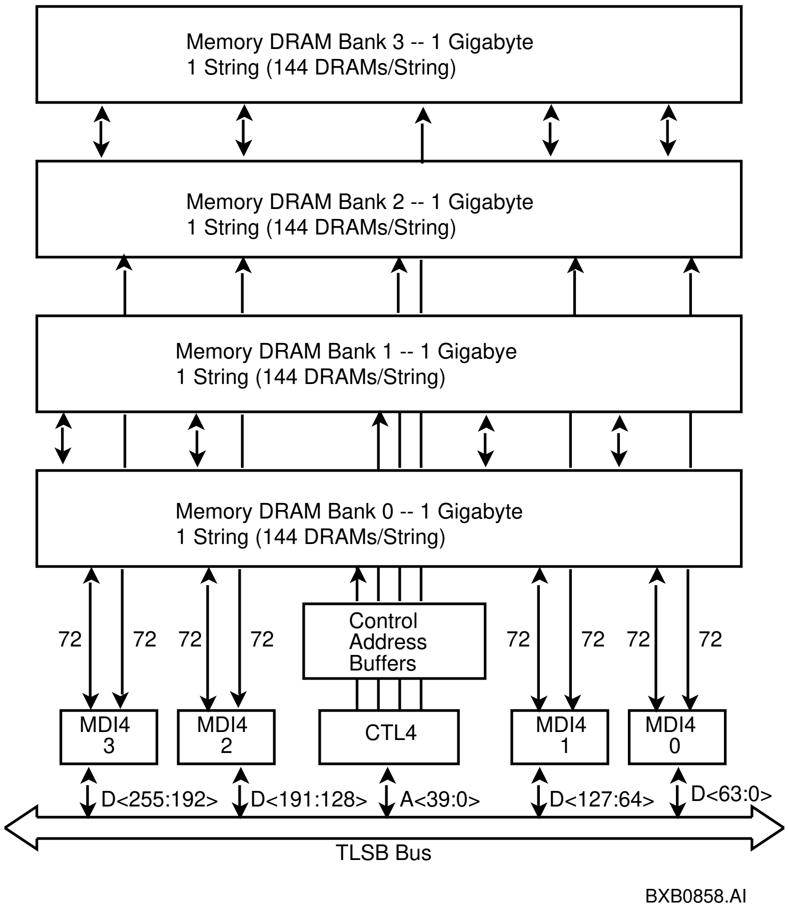
1.2 Major Sections

A TLSB memory module consists of three major sections:

- Control address interface (CTL4)
- Memory data interface (MDI4)
- DRAM arrays

The major sections communicate with each other through internal buses. Figure 1-1 shows a block diagram of the MS7CC-GA memory module.

Figure 1-1 MS7CC-GA Memory Module Block Diagram



1.2.1 Control Address Interface

The control address interface (CTL4) is a single gate array. It provides the interface to the TLSB, controls DRAM timing and refresh, runs memory self-test, and contains some of the TLSB and memory-specific registers.

CTL4 decodes the TLSB command and memory bank in the case of memory reads and writes, or the TLSB address during CSR operations to determine if it is selected for this transaction. In addition, command/address parity is checked to determine if a command/address parity error has occurred.

CTL4 contains the TLSB control sequencers responsible for the TLSB protocol.

CTL4 provides separate copies of Row/Column address, RAS, CAS, and WE signals for each of the four DRAM banks.

CTL4 controls the operation of the serial EEPROM on the memory module. The EEPROM contains the following information:

- The serial number of the module. This is entered into the EEPROM by manufacturing during module build.
- The module revision. This is entered into the EEPROM by manufacturing during module build. It is updated, as appropriate, anytime the module's revision changes.
- Self-test failures. If self-test fails, the console logs self-test failure data in the EEPROM.
- Memory module error logging data. This information is used to help diagnose and isolate failures on modules returned to a repair depot.

CTL4 interfaces to the TLSB command/address bus, which is independent from the data bus.

Internally, CTL4 consists of the following major functional areas:

- TLSB interface logic—command/address decode
- DRAM address generation logic for memory banks 0 through 3
- DRAM control signal timing logic for memory banks 0 through 3
- DRAM refresh control logic for memory banks 0 through 3
- CSRs
- Self-test address generation logic
- TLSB state machine control logic
- EEPROM control logic
- Control interface to the four MDI4 ASICs

1.2.2 Memory Data Interface

Each memory module has four memory data interface (MDI4) ASICs. Each MDI4 has a 72-bit interface to the TLSB and two 72-bit data interfaces to the DRAM arrays. The MDI4 includes data buffers, ECC checking logic, self-test data generation and checking logic, and CSRs.

MDI4 forwards two 72-bit TLSB transfers to the DRAMs during memory writes. During memory reads, two 72-bit transfers from the DRAMs are issued onto the TLSB.

For memory writes, each MDI4 contains four 144-bit write data buffers that are used to:

- Temporarily store the first data cycle (72 bits) from the TLSB until the second arrives and the write can be completed.
- Store all 144 bits, so that write data can be accepted off the TLSB independent of refresh or read operations to the other three banks, which may result in delaying the completion of the write from the memory's perspective.

For memory reads, each MDI4 contains four separate read buffers, one for each memory bank. Each read buffer can store 144 bits of read data. The read buffers perform several functions:

- Temporarily store the second TLSB data cycle for each memory bank, while the first is being output onto the TLSB bus.
- Store either one through four banks worth of read data, which is necessary if TLSB_HOLD is asserted, or if TLSB is very busy. Once RAS is asserted, the transaction MUST be completed.
- Contain "data-muxing" used to select between memory "fast-path" data, read buffer data, or CSR read data.

MDI4 contains the ECC checking logic that is used to check memory write data and memory read data to aid in system fault isolation. The ECC check bits are slightly modified before that data is written into the DRAMs by the addition of a Row and a Column parity bit. The purpose is to boost system data integrity in case of a single-bit Row or Column address failure. During memory reads, the modified ECC check bits are stripped of the Row/Column parity bits before data and check bits are driven onto the TLSB.

1.2.3 DRAM Arrays

The DRAM arrays consist of DRAMs, control signal, and address buffer components. The 4-Gbyte MS7CC-GA DRAM arrays are organized into four strings. Each string requires 144 DRAMs and is equivalent to one bank. The four 1-Gbyte banks are independently accessible. The MS7CC-GA memory modules use 16-Mbit deep x 4-bit wide DRAMs that are protected by a single-error correct, double-error detect quadword ECC code.

1.3 Memory Organization

The physical memory composed of a single or multiple memory modules can be organized in various ways to optimize memory access.

Memory can be configured with any mix of modules ranging in capacity from 128 Mbytes to the 4-Gbyte MS7CC-GA. The only restriction is that the total number of memory banks cannot exceed 16. Note that except for the MS7CC-GA, which has four memory banks but can be made to operate in a two-bank mode through a selection in the TLCNR register, all other memory modules have two banks of DRAM arrays. Table 1-1 lists the TLSB memory modules of various capacities.

Table 1-1 Memory Array Capacity

DRAM Type (Mbits)	Number of Strings	Memory Capacity (Mbytes)
4x1	2	128 (MS7CC-BA)
4x1	4	256 (MS7CC-CA)
4x1	8	512 (MS7CC-DA)
4x4	4	1024 (MS7CC-EA)
4x4	8	2048 (MS7CC-FA)
16x4	4	4096 (MS7CC-GA)

1.4 Memory Interleave

Memory performance is improved by interleaving the physical memory. Interleaving can be done at two levels: module and system.

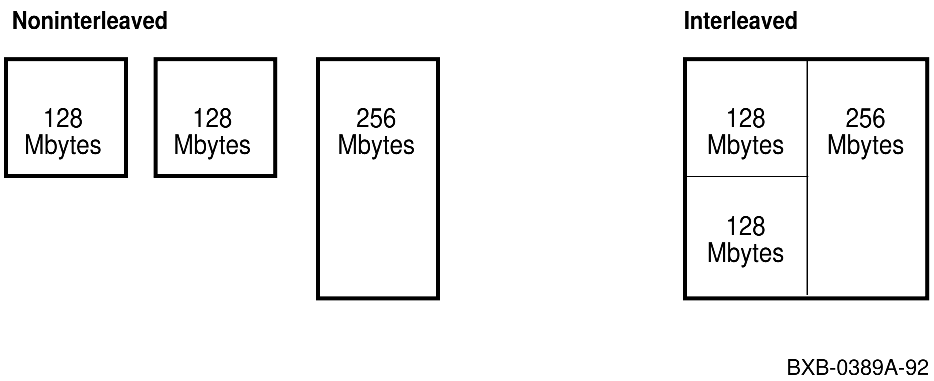
MS7CC-GA memory modules support 4-way interleaving.

A memory configuration on the TLSB consisting of 16 memory banks across '*n*' number of memory modules supports a maximum of 16-way interleaving.

Memory modules of different capacities can be interleaved as a set with modules of another capacity. For example, two 128-Mbyte modules can be interleaved with a single 256-Mbyte module as one set that is 4-way interleaved. This type of configuration yields 2-way module interleaving and 4-way system-level interleaving as shown in Figure 1-2. This same set can also be interleaved into a "pseudo 8-way" interleave set that will further boost system performance.

NOTE: For such a memory module set, the console configures memory to the "pseudo 8-way" interleave.

Figure 1-2 Interleaving Different Size Memory Modules



Interleaving of memory modules is set up by initialization software through mapping registers in TLSB commanders and in each memory module.

When memory modules are interleaved, each interleaved set is addressed on a 64-byte block boundary. In multiple interleaved modules, each consecutive 64-byte address targets the next memory module in the interleaved set. This is done because accessing multiple banks in one memory module can result in reduced system throughput due to common data path contention between the two banks.

1.5 Refresh

Each module implements CBR (CAS Before Ras) DRAM refresh. All memory modules refresh at the same time providing that a module is not servicing a TLSB memory transaction at the time when a refresh is requested. If a refresh request is asserted after a TLSB transaction has begun in a given memory bank, the TLSB transaction is completed and is followed immediately by the refresh operation.

In addition to refresh cycles during normal system operation, the MS7CC-GA refresh is initiated under power-up and system reset. Upon the deassertion of TLSB_RESET, the MS7CC-GA module initiates a start-up procedure that consists of:

- At least eight DRAM refresh cycles to initialize the DRAMS.
- All CSRs and required internal logic are set to a known initialized state.
- Self-test is initiated and run to completion.

Chapter 2

Registers

The MS7CC-GA registers are divided into two main groups:

- TLSB required registers
- Memory-specific registers

TLSB required registers are used for internode communications and transactions over the TLSB bus. Memory-specific registers implement functions related to the operation of the module.

All registers are located in node spaces and are accessed using CSR read or write commands. Nodes respond to all addresses within the node space. If a read is performed to a valid node, but to a CSR that is not implemented, the return data is Unpredictable.

2.1 Register Conventions

Certain conventions are followed in register descriptions and in references to bits and bit fields:

- Registers are referred to by their mnemonics, such as **TLCNR register.** The full name of a register (for example, **Memory Configuration Register**) is spelled out only at the top of the register description page, or when the register is first introduced.
- Bits and fields are enclosed in angle brackets. For example, **bit <31>** and **bits <31:16>**. For clarity of reference, bits are usually specified by their numbers or names enclosed in angle brackets adjacent to the register mnemonic, such as **TLBER<16>** or **TLBER<UDE>,** which are equivalent designations.
- When the value of a bit position is given explicitly in a register diagram, the information conveyed is as follows:

Bit Value Designation	Meaning
0	Reads as zero; ignored on writes.
1	Reads as one; ignored on writes.
X	Does not exist in hardware. The value of the bit is Unpredictable on reads and ignored on writes.

- The entry in the **type** column of a register description table may include the initialization value of the bits. For example, entry "R/W, 0" indicates a read/write bit that is initialized to 0.
- Acronyms are used throughout register descriptions to indicate the access type of the bit(s) as follows:

Acronym	Access Type
R	Read only; writes ignored.
R0	Read as zero.
R/W	Read/write.
U	Undefined
W	Write only.
W1C	Read/write one to clear; unaltered by a write of zero.
W1S	Write one to set; self-cleared; cannot be cleared by a write of zero.

2.2 Register Address Mapping

CSRs are mapped to a node space as offsets from a base address that is assigned to the node (slot on the TLSB backplane). The base address is implemented in hardware and depends on the node ID of the module, which is determined by the TLSB slot occupied by the module.

Table 2-1 gives the physical base addresses of nodes on the TLSB bus. Some registers are mapped to the broadcast space. The broadcast space base address (BSB) is common to all nodes and is FF 8E00 0000.

Table 2-1 TLSB Node Space Base Addresses

Node	Module	Physical Base Address (BB) Address Field <39:0> 34-Bit Range
0	CPU, Memory	FF 8800 0000
1	CPU, Memory	FF 8840 0000
2	CPU, Memory	FF 8880 0000
3	CPU, Memory	FF 88C0 0000
4	CPU, Memory, I/O	FF 8900 0000
5	CPU, Memory, I/O	FF 8940 0000
6	CPU, Memory, I/O	FF 8980 0000
7	CPU, Memory, I/O	FF 89C0 0000
8	I/O	FF 8A00 0000
Broadcast Space		FF 8E00 0000

2.3 TLSB Required Registers Implemented by Memory

Table 2-2 lists the TLSB registers implemented by memory. TLSB required CSR space spans a range of BB+0000–BB+0FC0.

Table 2-2 TLSB Required Memory Registers

Mnemonic	Name	Address	Implemented by
TLDEV	Device Register	BB+0000	CTL4
TLBER	Bus Error Register	BB+0040	CTL4
TLCNR	Configuration Register	BB+0080	CTL4
TLVID	Virtual ID Register	BB+00C0	CTL4
TLFADR0	TLSB Failing Address Register 0	BB+0600	CTL4
TLFADR1	TLSB Failing Address Register 1	BB+0640	CTL4
TLESR0	TLSB Error Syndrome Register 0	BB+0680	MDI4_0
TLESR1	TLSB Error Syndrome Register 1	BB+06C0	MDI4_1
TLESR2	TLSB Error Syndrome Register 2	BB+0700	MDI4_2
TLESR3	TLSB Error Syndrome Register 3	BB+0740	MDI4_3

2.4 Memory-Specific Registers

Table 2-3 lists the memory-specific registers. Memory-specific CSR space is reserved as follows:

- In CTL4: from BB+01800 to BB+0FFC0
- In MDI4_0: from BB+10000 to BB+13FC0
- In MDI4_1: from BB+14000 to BB+17FC0
- In MDI4_2: from BB+18000 to BB+1BFC0
- In MDI4_3: from BB+1C000 to BB+1FFC0

Table 2-3 Memory-Specific Registers

Mnemonic	Register Name	Address (Byte Offset)
Registers in CTL4		
SECR	Serial EEPROM Control/Data Register	BB[1] + 01800
MIR	Memory Interleave Register	BB + 01840
MCR	Memory Configuration Register	BB + 01880
MCR	Memory Configuration Register	BSB[2] + 01880
STAIR	Self-Test Address Isolation Register	BB + 018C0
STER	Self-Test Error Register	BB + 01900
MDRA	Memory Diagnostic Register A	BB + 01980
MDRB	Memory Diagnostic Register B	BB + 019C0
Registers in MDI4_0		
STDERA_0	Self-Test Data Error Register A_0	BB + 10000
STDERB_0	Self-Test Data Error Register B_0	BB + 10040
STDERC_0	Self-Test Data Error Register C_0	BB + 10080
STDERD_0	Self-Test Data Error Register D_0	BB + 100C0
STDERE_0	Self-Test Data Error Register E_0	BB + 10100
DDR0	Data Diagnostic Register 0	BB + 10140
Registers in MDI4_1		
STDERA_1	Self-Test Data Error Register A_1	BB + 14000
STDERB_1	Self-Test Data Error Register B_1	BB + 14040
STDERC_1	Self-Test Data Error Register C_1	BB + 14080
STDERD_1	Self-Test Data Error Register D_1	BB + 140C0
STDERE_1	Self-Test Data Error Register E_1	BB + 14100
DDR1	Data Diagnostic Register 1	BB + 14140
Registers in MDI4_2		
STDERA_2	Self-Test Data Error Register A_2	BB + 18000
STDERB_2	Self-Test Data Error Register B_2	BB + 18040
STDERC_2	Self-Test Data Error Register C_2	BB + 18080
STDERD_2	Self-Test Data Error Register D_2	BB + 180C0
STDERE_2	Self-Test Data Error Register E_2	BB + 18100
DDR2	Data Diagnostic Register 2	BB + 18140
Registers in MDI4_3		
STDERA_3	Self-Test Data Error Register A_3	BB + 1C000
STDERB_3	Self-Test Data Error Register B_3	BB + 1C040
STDERC_3	Self-Test Data Error Register C_3	BB + 1C080
STDERD_3	Self-Test Data Error Register D_3	BB + 1C0C0
STDERE_3	Self-Test Data Error Register E_3	BB + 1C100
DDR3	Data Diagnostic Register 3	BB + 1C140

[1] BB is the node space base address of the memory module in hex.

[2] BSB is the broadcast space base address, which is FF 8E00 0000. This register is write only.

TLDEV—Device Register

Address BB + 0000
Access R/W

The TLDEV register is loaded during initialization with information that identifies a node. A zero value indicates an uninitialized node.

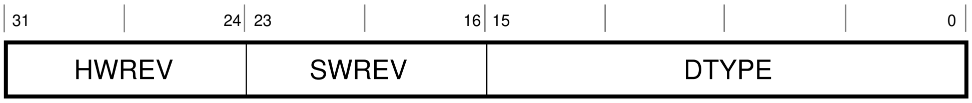


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Table 2-4 TLDEV Register Bit Definitions

Name	Bit(s)	Type	Function
HWREV	<31:24>	R/W, 0	**Hardware Revision.** Identifies the hardware revision level of a TLSB node. The value will be loaded by console firmware from information contained in the serial EEPROM. Bits <31:28> specify a major revision number and bits <27:24> specify a minor revision number to be displayed by the console in the format 0.0 through 15.15.
SWREV	<23:16>	R/W, 0	**Software Revision.** Identifies the software (or firmware) revision level of a TLSB node. The value will be loaded by console firmware from information contained in the serial EEPROM. Bits <23:20> specify a major revision number and bits <19:16> specify a minor revision number to be displayed by the console in the format 0.0 through 15.15. These bits shall be zero if a software revision level is not applicable to this node.
DTYPE	<15:0>	R/W, 0	**Device Type.** Identifies the type of node. Memory hardware loads a value of 5800 (hex) into this field upon power-up or reset.

TLBER—Bus Error Register

Address BB + 0040
Access R/W

The TLBER register contains bits that are set when a TLSB node detects errors in the TLSB system. The entire register is locked when the first error bit gets set in this register if TLCNR<LOFE> is set. All bits except the four DSn bits cause the register to be locked. When the register is locked, no bits change value until all bits are cleared by software or TLCNR<LOFE> is cleared. Locking the register is intended only for diagnostics. Not intended for use in normal operation.

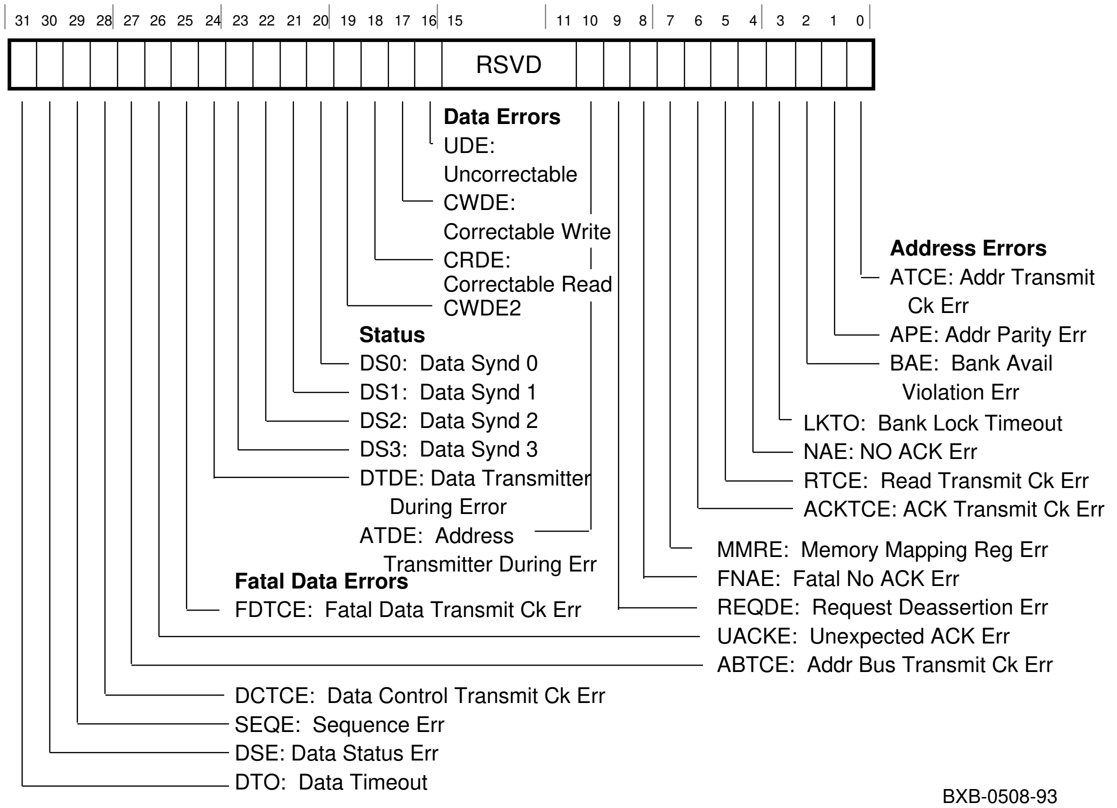

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Table 2-5 TLBER Register Bit Definitions

Name	Bit(s)	Type	Function
DTO	<31>	W1C, 0	**Data Timeout.** *Memory:* Not implemented.
DSE	<30>	W1C, 0	**Data Status Error.** Set when TLSB_STATCHK does not match the logical OR of TLSB_SHARED and TLSB_DIRTY. This is a system fatal error that asserts TLSB_FAULT.
SEQE	<29>	W1C, 0	**Sequence Error.** Set when an unexpected value of TLSB_SEQ<3:0> is received. This is a system fatal error that asserts TLSB_FAULT.
DCTCE	<28>	W1C, 0	**Data Control Transmit Check Error.** Set when a transmit check error is detected on TLSB_SEND_DATA, TLSB_SEQ<3:0>, TLSB_SHARED, TLSB_DIRTY, TLSB_HOLD, TLSB_STATCHK, or TLSB_DATA_ERROR signals. This is a system fatal error that asserts TLSB_FAULT.
ABTCE	<27>	W1C, 0	**Address Bus Transmit Check Error.** Set when a transmit check error is detected on TLSB_ARB_SUP, TLSB_LOCKOUT, or TLSB_BANK_AVL<15:0> signals. This is a system fatal error that asserts TLSB_FAULT.
UACKE	<26>	W1C, 0	**Unexpected Acknowledge.** Set if a node receives unexpected TLSB_CMD_ACK. This is a system fatal error that asserts TLSB_FAULT.
FDTCE	<25>	W1C, 0	**Fatal Data Transmit Check Error.** Set when a node detects a data transmit check error and does NOT detect any ECC error. This is a system fatal error that asserts TLSB_FAULT.
DTDE	<24>	W1C, 0	**Data Transmitter During Error.** A status bit set on receipt of TLSB_DATA_ERROR if node was the transmitter of the data during data bus transaction.
DS3	<23>	R, U	**Data Syndrome 3.** A status bit set when the TLESR3 register contains status relative to the current data error. This bit is undefined when CRDE, CWDE, and UDE are zero. It is overwritten on a second error of higher significance.

Table 2-5 TLBER Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
DS2	<22>	R, U	**Data Syndrome 2.** A status bit set when the TLESR2 register contains status relative to the current data error. This bit is undefined when CRDE, CWDE, and UDE are zero. It is overwritten on a second error of higher significance.
DS1	<21>	R, U	**Data Syndrome 1.** A status bit set when the TLESR1 register contains status relative to the current data error. This bit is undefined when CRDE, CWDE, and UDE are zero. It is overwritten on a second error of higher significance.
DS0	<20>	R, U	**Data Syndrome 0.** A status bit set when the TLESR0 register contains status relative to the current data error. This bit is undefined when CRDE, CWDE, and UDE are zero. It is overwritten on a second error of higher significance.
CWDE2	<19>	W1C, 0	**Second Correctable Write Data Error.** Set when a second CWDE error is received when <CWDE> is still set from the first error.
CRDE	<18>	W1C, 0	**Correctable Read Data Error.** Set when a CRECC error is set in any TLESRn register. This is a soft error that asserts TLSB_DATA_ ERROR if CRDD is not set in the TLCNR register.
CWDE	<17>	W1C, 0	**Correctable Write Data Error.** Set when a CWECC error is set in any TLESRn register. This is a soft error that asserts TLSB_DATA_ ERROR if CWDD is not set in the TLCNR register.
UDE	<16>	W1C, 0	**Uncorrectable Data Error.** Set when <UECC> is set in any TLESRn register. This is a hard error that asserts TLSB_DATA_ ERROR.
RSVD	<15:11>	R0	**Reserved.** Read as zero.
ATDE	<10>	W1C, 0	**Address Transmitter During Error.** *Memory:* Not implemented.
REQDE	<9>	W1C, 0	**Request Deassertion Error.** *Memory:* Not implemented.

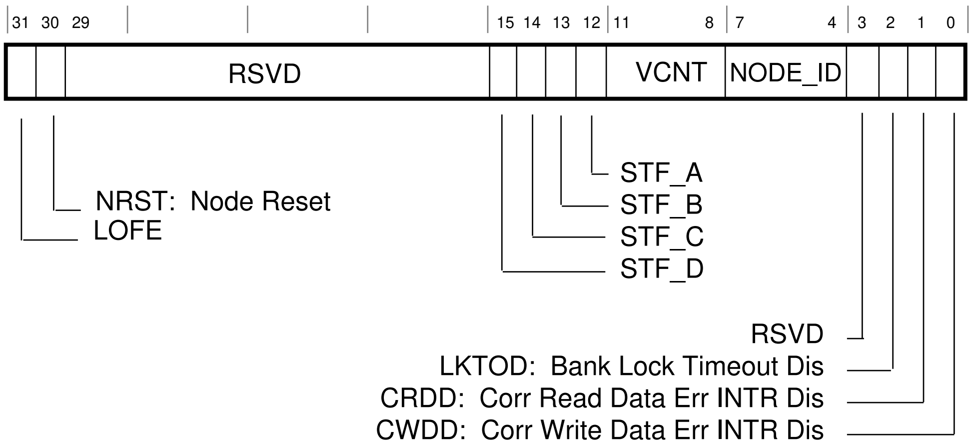
Table 2-5 TLBER Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
FNAE	<8>	W1C, 0	**Fatal No Acknowledge Error.** *Memory:* Not implemented.
MMRE	<7>	W1C, 0	**Memory Mapping Register Error.** *Memory:* Not implemented.
ACKTCE	<6>	W1C, 0	**Acknowledge Transmit Check Error.** Set when a transmit check error is detected on the TLSB_CMD_ACK signal. This is a system fatal error that asserts TLSB_FAULT.
RTCE	<5>	W1C, 0	**Request Transmit Check Error.** *Memory:* Not implemented.
NAE	<4>	W1C, 0	**No Acknowledge Error.** *Memory:* Not implemented.
LKTO	<3>	W1C, 0	**Bank Lock Timeout.** Set when a memory node times out waiting for a Write Bank Unlock command after processing a Read Bank Lock command. This is a hard error. The memory node asserts TLSB_BANK_AVL upon setting <LKTO>. This error is disabled if LKTOD is set in the TLCNR register.
BAE	<2>	W1C, 0	**Bank Available Violation Error.** Set when a memory bank is addressed by a memory access command while the memory bank is busy and has a TLSB_BANK_AVL signal asserted. Also set when any node detects a CSR access command while a CSR command is already in progress. This is a system fatal error that asserts TLSB_FAULT.
APE	<1>	W1C, 0	**Address Parity Error.** Set when a node detects even parity on the TLSB_ADR<30:5> and TLSB_ADR_PAR signals, or on the TLSB_ADR<39:31>, TLSB_ADR<4:3>, TLSB_BANK_NUM<3:0>, TLSB_CMD<2:0>, and TLSB_CMD_PAR signals. This is a system fatal error that asserts TLSB_FAULT.
ATCE	<0>	W1C, 0	**Address Transmit Check Error.** *Memory:* Not implemented.

TLCNR—Configuration Register

Address BB + 0080
Access R/W

The TLCNR register contains the TLSB system configuration setup and status information. Node-specific configuration information exists in node-specific registers.



BXB-0492B-96

Table 2-6 TLCNR Register Bit Definitions

Name	Bit(s)	Type	Function
LOFE	<31>	R/W, 0	**Lock on First Error.** If set, the node locks the TLBER and TLFADR registers when the first error bit is set in the TLBER register.
NRST	<30>	W, 0	**Node Reset.** When set, CSRs are reset to their initial states. Any transactions pending may be lost or left incomplete. Memory self-test halts if running and does NOT restart. An internally generated reset signal remains asserted for 32 TLSB bus cycles, which is sufficient to reset memory state and clear <NRST>.
RSVD	<29:20>	R0	**Reserved.** Read as zero.
RSVD	<19:16>	R1	**Reserved.** Read as ones.
STF_D	<15>	R/W, 1	**Self-Test Fail D.** When set, indicates that memory has not yet completed self-test. Memory clears this bit if self-test executes to completion **regardless of whether errors were found within the DRAM array.** When this bit is clear, the self-test LED will be lit, indicating that the module completed the self-test.
STF_C	<14>	R/W, 1	**Self-Test Fail C.** When set, indicates that memory has not yet completed self-test. Memory clears this bit if self-test executes to completion **regardless of whether errors were found within the DRAM array.** When this bit is clear, the self-test LED will be lit, indicating that the module completed the self-test.
STF_B	<13>	R/W, 1	**Self-Test Fail B.** When set, indicates that memory has not yet completed self-test. Memory clears this bit if self-test executes to completion **regardless of whether errors were found within the DRAM array.** When this bit is clear, the self-test LED will be lit, indicating that the module completed the self-test.
STF_A	<12>	R/W, 1	**Self-Test Fail A.** When set, indicates that memory has not yet completed self-test. Memory clears this bit if self-test executes to completion **regardless of whether errors were found within the DRAM array.** When this bit is clear, the self-test LED will be lit, indicating that the module completed the self-test.

Table 2-6 TLCNR Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
VCNT	<11:8>	R/W, 4	**Virtual Unit Count.** This field indicates the number of memory banks for which the MC7CC-GA is configured: VCNT = 4 (4 memory banks, 1 Gbyte each) VCNT = 2 (2 memory banks, 2 Gbytes each) The default mode is four memory banks, each one gigabyte in size (VCNT = 4). The TLSB can support a maximum of 16 memory banks. Seven MS7CC-GA memory modules, however, may have up to 28 separate memory banks. This would make it impossible to build a maximally configured memory system with MS7CC-GA memory modules. Writing a 2 hex in this field configures the MS7CC-GA memory module to two memory banks, each 2 Gbytes in size. In this configuration a maximum of seven MS7CC-GA memory modules (14 memory banks) may be installed on a single TLSB. The <VCNT> field should not be changed from the value set at system initialization when other bits in this register are modified.
NODE_ID	<7:4>	R, ID	**Node ID.** This field reflects the physical node ID as presented to the node by TLSB_NID<2:0>.
RSVD	<3>	R0	**Reserved.** Must be zero.
LKTOD	<2>	R/W, 0	**Bank Lock Timeout Disable.** When set, a memory node disables the timeout counter waiting for a Bank Unlock Write command after processing a Read Bank Lock command. The <LKTO> error bit in the TLBER register will not set.
CRDD	<1>	R/W, 0	**Correctable Read Data Error Interrupt Disable.** When set, TLSB_DATA_ERROR is not asserted on detection of a single-bit data error during a read command. Setting CRDD in all nodes disables correctable read data error interrupts.
CWDD	<0>	R/W, 0	**Correctable Write Data Error Interrupt Disable.** When set, TLSB_DATA_ERROR is not asserted on detection of a single-bit data error during a write command. Setting CWDD in all nodes disables correctable write data error interrupts.

TLVID—Virtual ID Register

Address BB + 00C0
Access R/W

The TLVID register contains the TLSB virtual identifiers assigned to a physical node. The virtual units can be CPUs or memory banks. The number of these units is presented in TLCNR<VCNT>. The units are addressed using virtual IDs that are assigned by writing the TLVID register.

CAUTION: This register must be loaded with a unique value for the virtual ID number of each memory bank, that is, no two of the VID_D, VID_C, VID_B, and VID_A fields are to be written with the same value. Otherwise, results of memory transactions will be unpredictable.

31 16	15 12	11 8	7 4	3 0
RSVD	VID_D	VID_C	VID_B	VID_A

BXB-0493A-96

Table 2-7 TLVID Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:16>	R, 0	**Reserved.** Read as zero.
VID_D	<15:12>	R/W, 0	**Virtual ID D.** *Memory:* Contains the virtual ID number for memory bank 3. Console loads this field at initialization time. The contents of this register are compared to TLSB_BANK_NUM <3:0> during a memory space command/address cycle to determine if bank 3 of this module is selected. This field must have a value different from any other VID_X field.
VID_C	<11:8>	R/W, 0	**Virtual ID C.** *Memory:* Contains the virtual ID number for memory bank 2. Console loads this field at initialization time. The contents of this register are compared to TLSB_BANK_NUM <3:0> during a memory space command/address cycle to determine if bank 1 of this module is selected. This field must have a value different from any other VID_X field.
VID_B	<7:4>	R/W, 0	**Virtual ID B.** *Memory:* Contains the virtual ID number for memory bank 1. Console loads this field at initialization time. The contents of this register are compared to TLSB_BANK_NUM <3:0> during a memory space command/address cycle to determine if bank 1 of this module is selected. This field must have a value different from any other VID_X field.
VID_A	<3:0>	R/W, 0	**Virtual ID A.** *Memory:* Contains the virtual ID number for memory bank 0. Console loads this field at initialization time. The contents of this register are compared to TLSB_BANK_NUM <3:0> during a memory space command/address cycle to determine if bank 0 of this module is selected. This field must have a value different from any other VID_X field.

TLFADRn—Failing Address Registers

Address BB + 0600, 0640
Access R/W

The TLFADRn registers contain status information associated with an error condition. Some nodes may not preserve this information for all error types. Therefore, field valid bits are used to indicate which fields contain data.

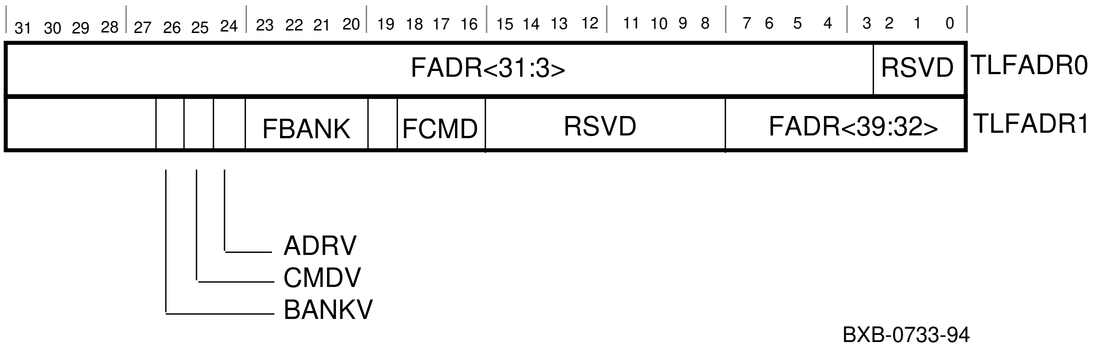


Table 2-8 TLFADRn Register Bit Definitions

Name	Bit(s)	Type	Function
TLFADR0			
FADR	<31:3>	R, U	**Failing Address<31:3>.** The address field from the command that resulted in an error. This field is Undefined when <ADRV> is zero.
RSVD	<2:0>	R0	**Reserved.** Must be zero.
TLFADR1			
RSVD	<31:27>	R0	**Reserved.** Must be zero.
BANKV	<26>	W1C, 0	**Bank Valid.** Set when <FBANK> contains a valid bank number from a bus transaction.
CMDV	<25>	W1C, 0	**Command Valid.** Set when <FCMD> contains a valid command code from a bus transaction.

Table 2-8 TLFADRn Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
TLFADR1			
ADRV	<24>	W1C, 0	**Address Valid.** Set when <FADR> contains a valid address from a bus transaction.
FBANK	<23:20>	R, U	**Failing Bank Number.** The bank number field from the command that resulted in an error. This field is Undefined when <BANKV> is zero.
RSVD	<19>	R0	**Reserved.** Reads as zero.
FCMD	<18:16>	R, U	**Failing Command Code.** The command code field from the command that resulted in an error. This field is Undefined when <CMDV> is zero.
RSVD	<15:8>	R0	**Reserved.** Read as zero.
FADR	<7:0>	R, U	**Failing Address<39:32>.** The high-order address field bits from the command that resulted in an error. This field is Undefined when <ADRV> is zero.

The TLFADRn registers are updated on the following conditions, listed in decreasing priority:

1. <APE>, <ATCE>, or TLBER<BAE> set in TLBER register
2. <UDE> sets in TLBER register
3. <CWDE> sets in TLBER register
4. <CRDE> sets in TLBER register

If any of the bits <ADRV>, <CMDV>, or <BANKV> are set, the registers are considered to be latched. A second occurrence of the same update condition does not overwrite latched status. However, latched status is overwritten if an update condition of higher priority occurs. The priority of each update condition is denoted by the number in the above list. A priority of 1 is the highest priority. When latched status is overwritten by a higher priority condition, all fields are updated, even if the update results in clearing <ADRV>, <CMDV>, or <BANKV>.

TLESRn—Error Syndrome Registers

Address BB + 0680 through 0740
Access R/W

The TLESRn registers contain the status information on a data error within a 64-bit slice of the data.

TLESR0 contains the error syndrome and status derived from TLSB_D<63:0> and TLSB_ECC<7:0>.

TLESR1 contains the error syndrome and status derived from TLSB_D<127:64> and TLSB_ECC<15:8>.

TLESR2 contains the error syndrome and status derived from TLSB_D<191:128> and TLSB_ECC<23:16>.

TLESR3 contains the error syndrome and status derived from TLSB_D<255:192> and TLSB_ECC<31:24>.

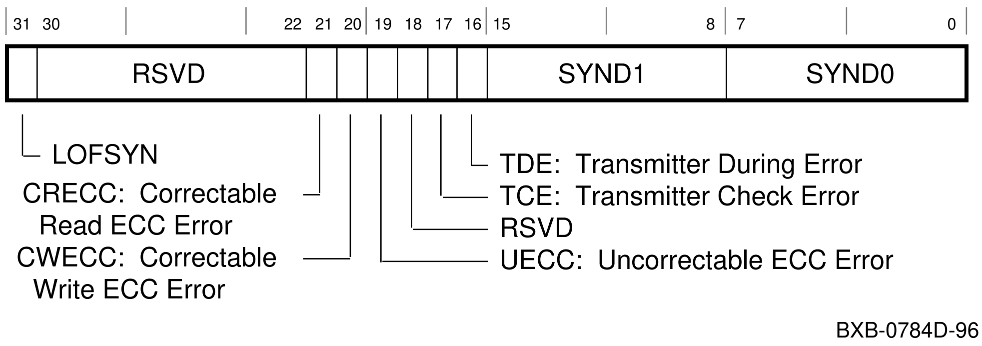


Table 2-9 TLESRn Register Bit Definitions

Name	Bit(s)	Type	Function
LOFSYN	<31>	R/W, 0	**Lock on First Syndrome.** When set, the TLESR register locks on the first error.
RSVD	<30:22>	R0	**Reserved.** Read as zero.
CRECC	<21>	W1C, 0	**Correctable Read ECC Error.** Set when an error occurs during a read command. This is a soft error.
CWECC	<20>	W1C, 0	**Correctable Write ECC Error.** Set when an error occurs during a write command. This is a soft error.
UECC	<19>	W1C, 0	**Uncorrectable ECC Error.** Set when an uncorrectable syndrome is detected, or if a correctable syndrome is detected on receipt of CSR data which the node is unable to correct. This is a hard error.
RSVD	<18>	R0	**Reserved.** Reads as zero.
TCE	<17>	W1C, 0	**Transmit Check Error.** Set when a transmit check error is detected on the TLSB_D or TLSB_ECC signals covered by the TLESRn register. This is a system fatal error if not accompanied by another error in this register (CRECC, CWECC, or UECC).
TDE	<16>	W1C, 0	**Transmitter During Error.** A status bit set when data transmitted by a node results in error. This bit is Undefined when <CRECC>, <CWECC>, and <UECC> are zero.
SYND1	<15:8>	R, U	**Syndrome 1.** Latched error syndrome from second data cycle. This field is Undefined when <CRECC>, <CWECC>, and <UECC> are zero.
SYND0	<7:0>	R, U	**Syndrome 0.** Latched error syndrome from first data cycle. This field is Undefined when <CRECC>, <CWECC>, and <UECC> are zero.

The four TLESRn registers are independent of each other. Each register displays error and status information on one 64-bit slice of data. Two consecutive data cycles of the 64-bit data slice constitute one data transaction. When an error is detected on the data bus, error bits may set in one or more TLESRn registers.

Multiple error bits may be set from a single data transaction. For example, <TCE> and <UECC> may both set at the same time. If <LOFSYN> is not set, multiple error occurrences cumulatively set error bits. The <TDE>, <SYND0>, and <SYND1> status bits present information from one data transaction. The data transaction for which status is presented is the first transaction that resulted in the most significant error type. The error types, in order of significance, are:

1. UECC—Hard error
2. CWECC—Soft error during write command
3. CRECC—Soft error during read command

If a CRECC error occurs in one data transaction, then a CWECC error in a later data transaction (and <LOFSYN> is not set), the <TDE>, <SYND0>, and <SYND1> fields change to reflect the status at the time of the CWECC error. If UECC is set, the status is latched and will not be changed no matter how many other error bits set later. Software must clear the error bits after each error to ensure proper reporting of the next error.

The <TDE>, <SYND0>, and <SYND1> fields are not latched due to TCE error. However, they will be latched if a TCE error also resulted in a correctable or uncorrectable ECC error.

A zero syndrome is the expected no error condition. A nonzero ECC syndrome may indicate a single-bit or a multiple-bit error.

Four error bits in the TLBER register will set as a result of the five error bits in this register.

- CRECC sets TLBER<CRDE>
- CWECC sets TLBER<CWDE>
- UECC sets TLBER<UDE>
- TCE, when no ECC error detected, sets TLBER<FDTCE>

The TLBER register also records which TLESRn registers contain status for the most significant error by setting the <DSn> bits accordingly.

SECR—Serial EEPROM Control/Data Register

Address BB + 0000 1800
Access R/W

The SECR register is used to access the EEPROM on the memory module. Access to the EEPROM is accomplished by continual updates of this register by software.

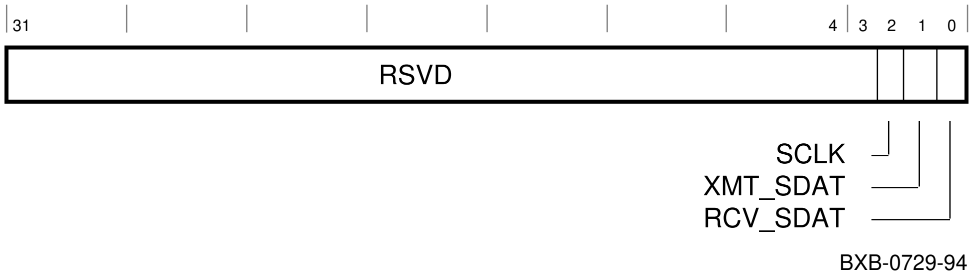


Table 2-10 SECR Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:3>	R0	**Reserved.** Read as zero.
SCLK	<2>	R/W, 0	**Serial Clock.** Used to implement the EEPROM serial clock interface by software. When this bit is written with a one, the EEPROM serial clock input is forced to a logic high. When this bit is cleared, the serial clock input is forced to low logic level.
XMT_SDAT	<1>	R/W, 1	**Transmit Serial Data.** Used by software to assert the serial data line of the EEPROM to either high or low logic levels. This bit is used with the SCLK bit to transfer command, address, and write data to the EEPROM. Must be set to one to receive an EEPROM response or serial read data.
RCV_SDAT	<0>	R	**Receive Serial Data.** Returns the status of the EEPROM serial data line. This bit is used by software to receive serial read data and EEPROM responses.

MIR—Memory Interleave Register

Address BB + 0000 1840
Access R/W

The MIR register is used by memory to determine DRAM RAS selection based upon how a given memory module is configured on the TLSB. Console software initializes this register upon start-up after system or node reset.

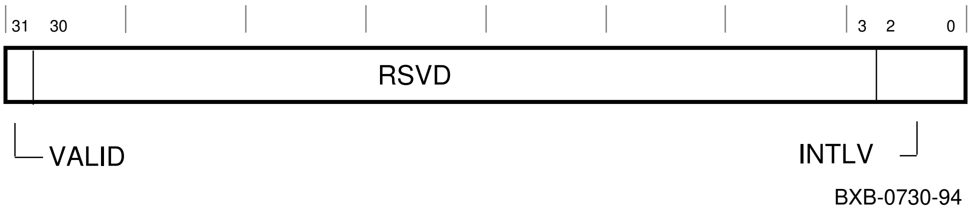


Table 2-11 MIR Register Bit Definitions

Name	Bit(s)	Type	Function
VALID	<31>	R/W, 0	**Valid.** When set, enables the module to respond to TLSB memory space transactions.
RSVD	<30:3>	R0	**Reserved.** Read as zero.
INTLV	<2:0>	R/W, 0	**Interleave.** The value of this field loaded by console during system initialization determines whether this module is 1, 2, 4, 8, or 16-way interleaved in the system.

INTLV (Hex)	Banks/ Module	No. of Modules	Interleave
0	1	1	1-way
0	2	1	Reserved
0	4	1	Reserved
1	1	2	2-way
1	2	1	2-way
1	4	1	Reserved
2	1	4	4-way
2	2	2	4-way
2	4	1	4-way
3	1	8	8-way
3	2	4	8-way
3	4	2	8-way
4	2	8	16-way
4	4	4	16-way
5,6,7,			Reserved

MCR—Memory Configuration Register

Address BB + 0000 1880; BSB + 0000 1880
Access R/W

The MCR register provides information about the DRAM array structure including DRAM type and number of strings installed. This information is required by the console to set up the eight address mapping registers in each TLSB commander node and the MIR register located on each memory module. The MCR register also contains a 2-bit field (DTR) that is used to select one of three cycle time variants.

A unique feature of this register is that it responds to a TLSB broadcast space address (BSB+1880). This feature allows all memory modules to set the DRAM timing rate at the same time. This feature is important to ensure that all memory modules continue to refresh at the same time whenever MCR<DTR> is updated.

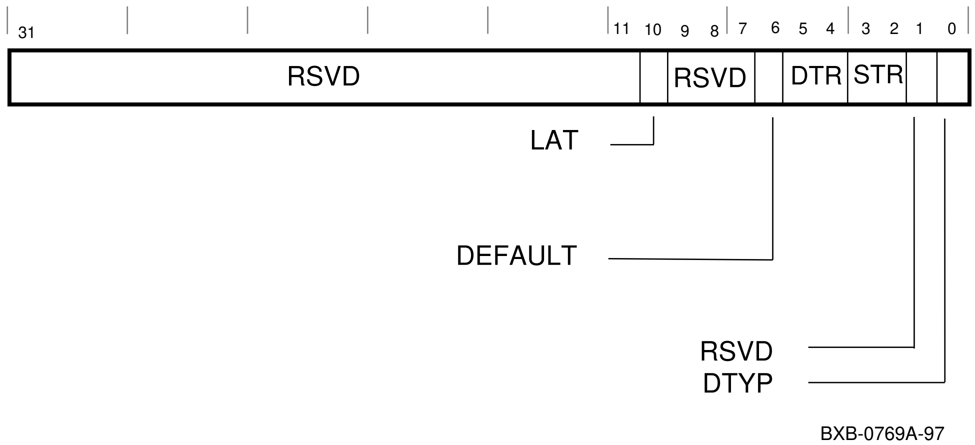


Table 2-12 MCR Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:11>	R0	**Reserved.** Read as zero.
LAT	<10>	R/W, 0	**Reduced Latency.** When set, reduces the DRAM read latency by one cycle and the DRAM write cycle time by one cycle. As a result, about a 5% performance gain is realized. This bit should be set only on systems running at TLSB bus cycle times of 11.0 ns or slower.
RSVD	<9:7>	R0	**Reserved.** Read as zero.
DEFAULT	<6>	W1C, 1	**Default Power-Up State.** When set, indicates that the memory's DRAM timing rate and refresh rate are set to the default power-up or reset values. Writing the <DTR> field to **any value** clears this bit. This bit is normally set on power-up or reset.

Table 2-12 MCR Register Bit Definitions (Continued)

<table>
<tr><th>Name</th><th>Bit(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>DTR</td><td><5:4></td><td>R/W, 11</td><td>DRAM Timing Rate. This field is used to modify the DRAM timing and refresh rate. At reset, DRAM refresh rate defaults to supporting a 15 ns bus (refresh counter equals 1008 bus cycles). <DTR> is normally written by console through a TLSB broadcast write command. This ensures that all memories will remain syncronized as to when they refresh the DRAMs. The <DTR> field should not be changed from the value set by console when other bits in this field are modified.

The following table gives the recommended refresh rate settings for different TLSB bus speeds.

<table>
<tr><th><DTR></th><th>Bus Speed Range</th><th>Refresh Counter Value</th></tr>
<tr><td>00</td><td>10.0 - 11.2</td><td>1360</td></tr>
<tr><td>01</td><td>Reserved</td><td>None</td></tr>
<tr><td>10</td><td>11.3 - 12.9</td><td>1088</td></tr>
<tr><td>11</td><td>13.0 - 15.0</td><td>1008 (Default)</td></tr>
</table></td></tr>
<tr><td>STR</td><td><3:2></td><td>R, 10</td><td>Strings Installed. This field supplies information about the number of strings installed on a module. The MS7CC-GA has four strings (<STR>=10).

<table>
<tr><th>STR</th><th>Strings</th></tr>
<tr><td>00</td><td>1</td></tr>
<tr><td>01</td><td>2</td></tr>
<tr><td>10</td><td>4</td></tr>
<tr><td>11</td><td>8</td></tr>
</table></td></tr>
<tr><td>RSVD</td><td><1></td><td>R0</td><td>Reserved. Read as zero.</td></tr>
<tr><td>DTYP</td><td><0></td><td>R, 0</td><td>DRAM Type. This field supplies information about what size DRAM technology is being used; this together with the number of strings installed determines module capacity.

<table>
<tr><th>DTYP</th><th>DRAM Type</th></tr>
<tr><td>0</td><td>64 Mbit</td></tr>
<tr><td>1</td><td>256 Mbit</td></tr>
</table></td></tr>
</table>

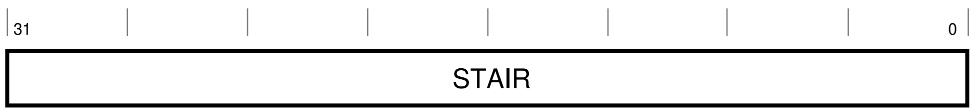
STAIR—Self-Test Address Isolation Register

Address BB + 0000 18C0
Access R/W

The STAIR register is used to isolate self-test failures to a given address segment or segments in the case of multiple failures in a module. This register breaks up a memory module into 32 distinct address segments. Each segment maps 128 Mbytes (2 meg 64-byte blocks) of memory. When a bit is set following completion of self-test, the corresponding address segment has failed. This information can be used by the console to map out bad areas of memory. Address segments are mapped according to total possible MS7CC-GA module capacity (four strings and 4-Gbyte capacity). The contents of this register will be cleared when bit <7> (POEMC) in the MDRA register is asserted while self-test is executed in POEM mode.

NOTE: Each bit in the STAIR register maps only 32 Mbytes of memory in one specific memory bank as bad. However, when the memory is 4-way interleaved, 128 Mbytes (32 Mbytes from each of the four memory banks) must be mapped out.

It is recommended that 32 Mbytes from each memory bank always be mapped out, regardless of the actual failing bank or the memory module's interleave mode.



BXB-0732-93

Table 2-13 STAIR Register Bit Definitions

Name	Bit(s)	Type	Function
STAIR	<31:0>	W1C, 0	**Self-Test Failing Address Range.** A bit in this register is set when self-test detects a data mismatch error in the corresponding address segment. The address range specified in Table 2-14 indicates the failing address segment.

Address segments are mapped according to total *possible* module capacity (maximum of 8 strings 2-Gbyte capacity), not to the capacity implemented, which may be less. In Table 2-14 all addresses are listed as physical byte addresses.

Table 2-14 STAIR Register Bit Correspondence of Memory Address Segments

Bit Set	Failing Address Range	Bit Set	Failing Address Range
0	0000 0000 – 07FF FFFF	16	8000 0000 – 87FF FFFF
1	0800 0000 – 0FFF FFFF	17	8800 0000 – 8FFF FFFF
2	1000 0000 – 17FF FFFF	18	9000 0000 – 97FF FFFF
3	1800 0000 – 1FFF FFFF	19	9800 0000 – 9FFF FFFF
4	2000 0000 – 27FF FFFF	20	A000 0000 – A7FF FFFF
5	2800 0000 – 2FFF FFFF	21	A800 0000 – AFFF FFFF
6	3000 0000 – 37FF FFFF	22	B000 0000 – B7FF FFFF
7	3800 0000 – 3FFF FFFF	23	B800 0000 – BFFF FFFF
8	4000 0000 – 47FF FFFF	24	C000 0000 – C7FF FFFF
9	4800 0000 – 4FFF FFFF	25	C800 0000 – CFFF FFFF
10	5000 0000 – 57FF FFFF	26	D000 0000 – D7FF FFFF
11	5800 0000 – 5FFF FFFF	27	D800 0000 – DFFF FFFF
12	6000 0000 – 67FF FFFF	28	E000 0000 – E7FF FFFF
13	6800 0000 – 6FFF FFFF	29	E800 0000 – EFFF FFFF
14	7000 0000 – 77FF FFFF	30	F000 0000 – F7FF FFFF
15	7800 0000 – 7FFF FFFF	31	F800 0000 – FFFF FFFF

Each module executes self-test as if it were the only memory module in the system (no interleave with other modules).

Assuming a given processor takes approximately 600 nanoseconds to scan each 64-byte block of memory for uncorrectable ECC errors, a 128-Mbyte failing address segment will take about 1.2 seconds to scan from the first to the last block.

STER—Self-Test Error Register

Address BB + 0000 1900
Access R/W

The STER register contains address information pertaining to data mismatch failures while self-test executes in POEM (pause on error) mode. The contents of this register when read after an error has been detected in POEM mode can be used to isolate the failing DRAM string and to indicate which of the four MDI4s the error was detected in. This information in conjunction with the four STDERA:E registers located in the MDI4 ASICs can be used to isolate down to a failing DRAM bit or bits. This register is cleared when MDRA<POEMC> is asserted.

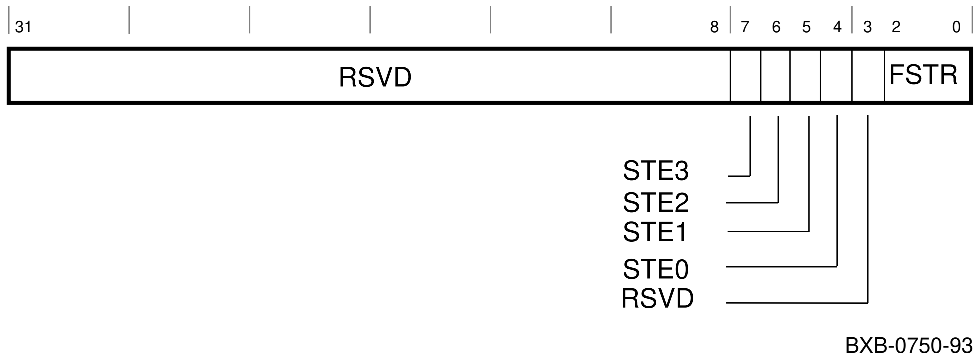


Table 2-15 STER Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:8>	R0	**Reserved.** Read as zero.
STE3	<7>	W1C, 0	**Self-Test Error in MDI4_3.** Set during POEM mode when MDI4_3 detects a data mismatch error. The setting of this bit locks bit <6> (STE2), bit <5> (STE1), bit <4> (STE0), and bits <2:0> (FSTR) of the failing string field[1].
STE2	<6>	W1C, 0	**Self-Test Error in MDI4_2.** Set during POEM mode when MDI4_2 detects a data mismatch error. The setting of this bit locks bit <7> (STE3), bit <5> (STE1), bit <4> (STE0), and bits <2:0> (FSTR) of the failing string field[1].
STE1	<5>	W1C, 0	**Self-Test Error in MDI4_1.** Set during POEM mode when MDI4_1 detects a data mismatch error. The setting of this bit locks bit <7> (STE3), bit <6> (STE2), bit <4> (STE0), and bits <2:0> (FSTR) of the failing string field[1].
STE0	<4>	W1C, 0	**Self-Test Error in MDI4_0.** Set during POEM mode when MDI4_0 detects a data mismatch error. The setting of this bit locks bit <7> (STE3), bit <6> (STE2), bit <5> (STE1), and bits <2:0> (FSTR) of the failing string field[1].
RSVD	<3>	R0	**Reserved.** Read as zero.
FSTR	<2:0>	R	**Failing String.** When read together with the <STEx> bits, this field indicates the failing DRAM string when a data mismatch error is detected by self-test. This field is Undefined if none of the <STEx> bits are set.

[1] Any one STER bit being set will prevent the other STER bits from being set on a subsequent data mismatch during self-test. More than one STER bit may be set if multiple MDI ASICs detect a data mismatch during the same cycle. A data mismatch error is defined as any failure that is detected within a 64-byte block that is considered to be a bus transaction.

MDRA—Memory Diagnostic Register A

Address BB + 0000 1980
Access R/W

MDRA register A is used by diagnostics and manufacturing to force error conditions in the memory module and isolate failures.

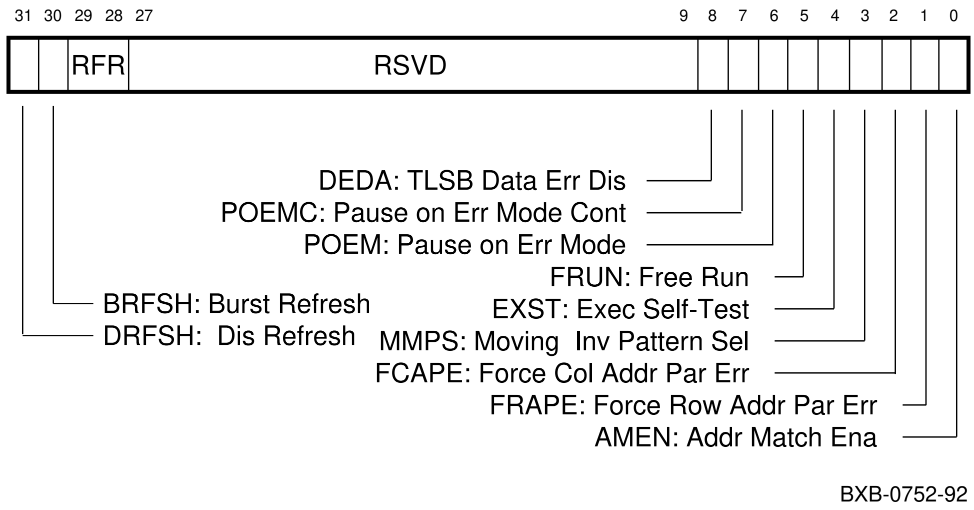


Table 2-16 MDRA Register Bit Definitions

Name	Bit(s)	Type	Function
DRFSH	<31>	R/W, 0	**Disable Refresh.** When set, "on-board" refresh of the module is disabled and diagnostic burst refresh, bit <30>, is enabled. When this bit is set concurrently with bit <30>, a burst refresh cycle will be executed.
BRFSH	<30>	W, 0	**Burst Refresh.** When set, and bit <31> is also set, a single row address within the addressed DRAMs will be refreshed as per CAS before RAS refresh operation. When this bit is set concurrently with bit <31>, a burst refresh cycle is executed.

Table 2-16 MDRA Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
RFR	<29:28>	R/W, 00	**Refresh Rate.** Determines the refresh rate of the module. <RFR> / Refresh Rate: 00 — 1X (Default) 01 — 2X 10 — 4X 11 — Reserved
RSVD	<27:9>	R0	**Reserved.** Read as zero.
DEDA	<8>	R/W, 0	**TLSB_DATA_ERROR Disable.** When set and used in conjunction with POEM or FRUN modes, TLSB_DATA_ERROR will not assert if an error is detected. This bit would be set by a user that wishes to run POEM or FRUN self-test modes in a system environment (console mode) where the assertion of TLSB_DATA_ERROR would prevent the system from operating correctly.
POEMC	<7>	W, 0	**Pause on Error Mode Continue.** When set in conjunction with <POEM> and <EXST> of this register, causes memory self-test to continue executing from the point where it halted due to an error condition being detected. At this point self-test will either halt on the next error, or continue to loop. <EXST> is cleared by software, when TLSB_RESET is asserted or <NRST> is set. When asserted following an error detection, the STER and STAIR registers are cleared. This bit is only valid when self-test is in POEM mode. Setting this bit during other self-test modes results in Undefined operation.[1,2]

[1] If <POEM> is set and an error occurs on Bank0 of two back-to-back reads in modules of greater than one string, an error detected on the second read to Bank1 will not be reported.

[2] When an error is detected during POEM mode, the data bit(s) in error will be logged in the STDERA,B,C,D,E registers in each MDI4 ASIC. Since the assertion of POEMC will not clear the error bits in the STDERA:E registers, it is required that the user set bit <1> in DDR0:3 prior to setting <POEMC>.

Table 2-16 MDRA Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
POEM[1]	<6>	R/W, 0	**Pause on Error Mode.** When set, self-test will halt execution upon the detection of a data mismatch error. TLSB_DATA_ERROR is asserted and remains asserted providing that <DEDA> is cleared, until either <POEM> is set or the module is reset. This bit is used in conjunction with <EXST> to execute self-test in this mode. When set, self-test continues to loop until <EXST> is cleared by software, when TLSB_RESET is asserted or <NRST> is set.
FRUN	<5>	R/W, 0	**Free Run.** When set in conjunction with <EXST>, memory will continue to loop on self-test until <EXST> is cleared, TLSB_RESET is asserted, or Node Reset is asserted. If while operating in Free Run mode, self-test detects a data mismatch, TLSB_DATA_ERROR will assert and remain asserted providing that DEDA is cleared, until either FRUN is cleared or the module is reset. Setting this bit in conjunction with other self-test modes results in Undefined operations.
EXST	<4>	R/W, 1	**Execute Self-Test.** When set, and the DRAM option mode is selected, memory self-test is invoked. The self-test logic examines this bit and bits <10:9> in MCR to determine if self-test should be executed. If the option field is zero, self-test does not execute. This bit is set upon system power-up or TLSB_RESET.
MMPS	<3>	R/W, 0	**Moving Inversion Pattern Select.** When set, memory self-test executes a specific moving inversion test pattern that combines specific data and address test patterns known to detect DRAM sensitivity faults. This bit must be selected in conjunction with bit <3> (Self-Test Pattern Select) in DDR0:3 registers to execute this special test. This mode is normally selected only during memory manufacturing.

[1] Lock on Error (LOE) in the four Data Diagnostic Registers (DDR0:3) must be set prior to executing self-test in POEM mode. This ensures that the Self-Test Data Error registers capture the first failure only.

Table 2-16 MDRA Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
FCAPE	<2>	R/W, 0	**Force Column Address Parity Error.** When set, incorrect DRAM column address parity is written into the addressed location when a match is detected between the TLSB address and the MDRB register and when <AMEN> is also set.
FRAPE	<1>	R/W, 0	**Force Row Address Parity Error.** When set, incorrect DRAM row address parity is written into the addressed location when a match is detected between the TLSB address and the MDRB register and when <AMEN> is also set.
AMEN	<0>	R/W, 0	**Address Match Enable.** When set, a TLSB memory space address or a self-test generated address is matched against the 32-bit 64-byte aligned address contained in MDRB. If a match is detected, and if bit 15, <EFLPD>, and/or bit 14, <EFLPC>, in one or all of the DDR0:3 registers are also set, then the data bit and/or check bit selected to be flipped during a memory space write will be written to memory inverted. In addition to the above, AMEN is also used to enable address match comparisons to force ROW and COL parity errors.

MDRB—Memory Diagnostic Register B

Address BB + 0000 19C0
Access R/W

Memory Diagnostic Register B contains a 32-bit 64-byte aligned address value that is directly compared to TLSB_ADR<37:6>, or an address generated by the self-test address generator. The value loaded into this register is used in conjunction with MDRA and DDR0:3 to cause a specific data bit and/or check bit to be flipped whenever a TLSB memory write address matches the value contained in this register.

NOTE: Since the TLSB addresses are 64-byte aligned, only TLSB_ADR<37:6> need be compared with this register. TLSB_ADR<4:0> is not used and TLSB_ADR<5> is the WRAP bit, which is ignored in the comparison.

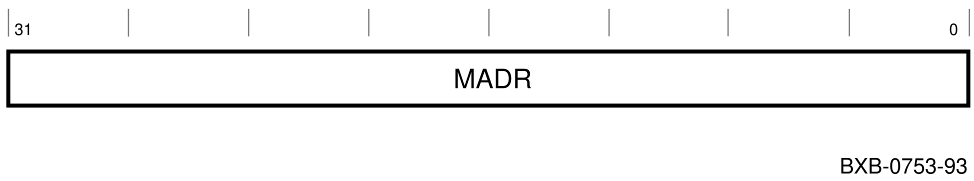


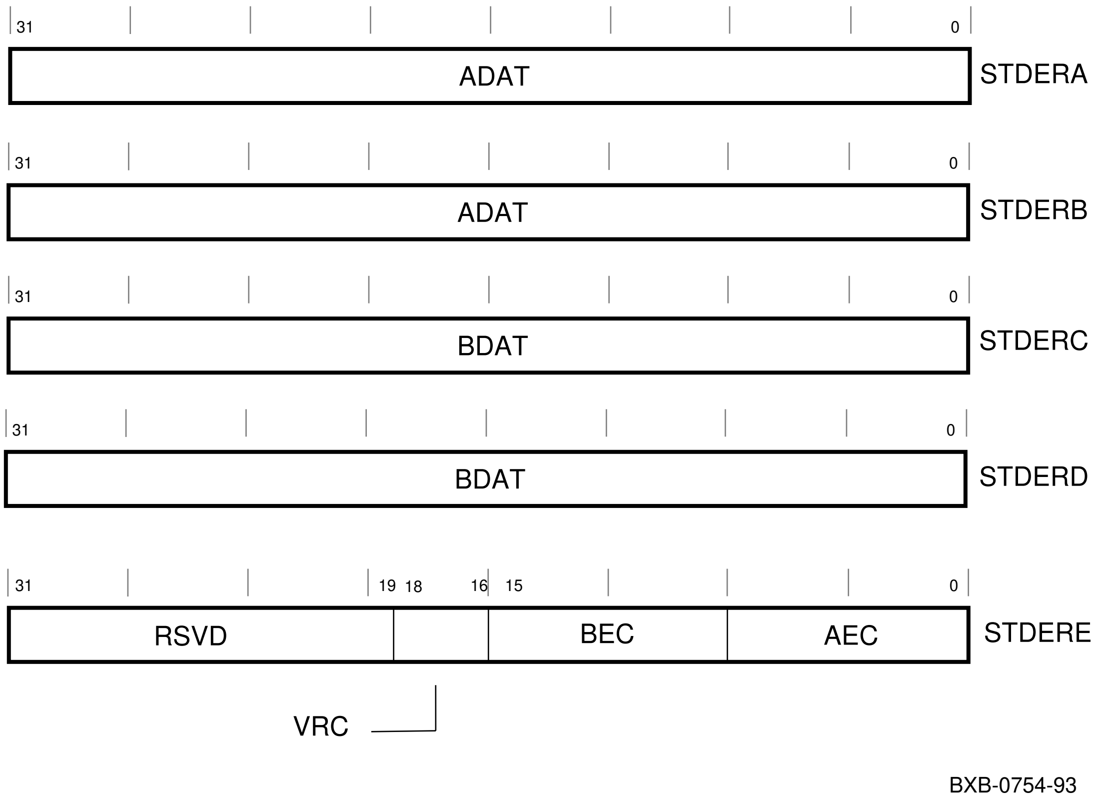
Table 2-17 MDRB Register Bit Definitions

Name	Bit(s)	Type	Function
MADR	<31:0>	R/W, 0	**Match Address.** The register may be loaded with an address value that is used in diagnostic modes to cause correctable and uncorrectable ECC errors to be written to memory at the 128-byte aligned address contained in this field.

STDERA,B,C,D,E—Self-Test Data Error Registers

Address BB + 0001 0000 to 0001 C100
Access R/W

The four sets of STDERx_n registers are used to isolate self-test failures down to a single failing bit or bits. When self-test is executed any data bit error(s) that are detected by the self-test data compare logic will set the appropriate data bit(s) in these registers. The operation and contents of this register can be affected by bits <2:0> of the DDR0:3 registers in the MDI4 ASICs.



ADAT = Data bits, TLSB DATA CYCLE_0/SYND0 in TLESRn.
BDAT = Data bits, TLSB DATA CYCLE_1/SYND1 in TLESRn.
AEC = Check bits, TLSB DATA CYCLE_0/SYND0 in TLESRn.
BEC = Check bits, TLSB DATA CYCLE_1/SYND1 in TLESRn.

The function of STDERA is slightly different from the other four registers (STDERB,C,D,E). STDERA can be written or read, while the other four are read only. STDERA can be used by diagnostics to ensure that most of the data path and control logic, to and from the various CSRs, is fully functional.

Table 2-18 describes each field of self-test error data registers A,B,C,D. These four registers are used to store failing self-test data bits <127:0> in MDI4_0, <255:128> in MDI4_1, <383:256> in MDI4_2, and <511:384> in MDI4_3.

Table 2-18 STDER A, B, C, D Register Bit Definitions

Name	Bit(s)	Type	Function
STDERA	<31:0>	R/W, 0	**Self-Test Data Error Register A.** One or more bits set indicate a self-test data bit error. The contents of this register can be used to isolate self-test failures to a single failing bit. This register can be read or written as an aid in determining proper CSR operation.
STDERB	<31:0>	R, 0	**Self-Test Data Error Register B.** One or more bits set indicate a self-test data bit error. The contents of this register can be used to isolate self-test failures to a single failing bit.
STDERC	<31:0>	R, 0	**Self-Test Data Error Register C.** One or more bits set indicate a self-test data bit error. The contents of this register can be used to isolate self-test failures to a single failing bit.
STDERD	<31:0>	R, 0	**Self-Test Data Error Register D.** One or more bits set indicate a self-test data bit error. The contents of this register can be used to isolate self-test failures to a single failing bit.

Table 2-19 describes each field of self-test data error register E. This register is used to store failing self-test ECC check bits <15:0> in MDI4_0, <31:16> in MDI4_1, <47:32> in MDI4_2, and <63:48> in MDI4_3.

The operation and contents of this register can be affected by bits <2:0> of the DDR0:3 registers in the MDI4 ASICs.

Table 2-19 STDERE Register Bit Definitions

<table>
<tr><th>Name</th><th>Bit(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>RSVD</td><td><31:20></td><td>R0</td><td>Reserved. Read as zero.</td></tr>
<tr><td>VRC</td><td><19:16></td><td>R, X</td><td>Valid Residue Check. This 4-bit read-only field is loaded at the beginning of the third pass in self-test and specifies which one of eight values will be used by the self-test data-checking logic to determine that the self-test data linear feedback shift register logic is working correctly. This field is useful in diagnosing improper operation of self-test that may be due to a faulty module or ASIC. The value read from this register is based upon the DRAM type and the number of strings on a given module. This field is Undefined in moving inversion self-test mode.

NOTE: VRC is always 7 for the 4-Gbyte MS7CC-GA module.

<table>
<tr><th>VRC (Hex)</th><th>DRAM Type</th><th>No. of Strings</th><th>Module Capacity (Mbyte)</th></tr>
<tr><td>0</td><td>4 Mbit</td><td>1</td><td>64 (N/A)</td></tr>
<tr><td>1</td><td>4 Mbit</td><td>2</td><td>128</td></tr>
<tr><td>2</td><td>4 Mbit</td><td>4</td><td>256</td></tr>
<tr><td>3</td><td>4 Mbit</td><td>8</td><td>512</td></tr>
<tr><td>4</td><td>16 Mbit</td><td>1</td><td>256</td></tr>
<tr><td>5</td><td>16 Mbit</td><td>2</td><td>512</td></tr>
<tr><td>6</td><td>16 Mbit</td><td>4</td><td>1024</td></tr>
<tr><td>7</td><td>16 Mbit</td><td>8</td><td>2048</td></tr>
<tr><td>7</td><td>64 Mbit</td><td>4</td><td>4096</td></tr>
<tr><td>9-15</td><td>Reserved</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>STDERE</td><td><15:0></td><td>R, 0</td><td>Self-Test Data Error Register_E. One or more bits set indicate a self-test data ECC check bit error. The contents of this register can be used to isolate self-test failures to a single failing bit.</td></tr>
</table>

DDR0:3—Data Diagnostic Registers

Address BB + 0001 0140; 0001 04140; 0001 8140; 0001 C140
Access R/W

There are four DDR registers, one in each of the four MDI ASICs. They are used by diagnostics and manufacturing to force error conditions, to isolate failures, and to margin the DC to DC power converters.

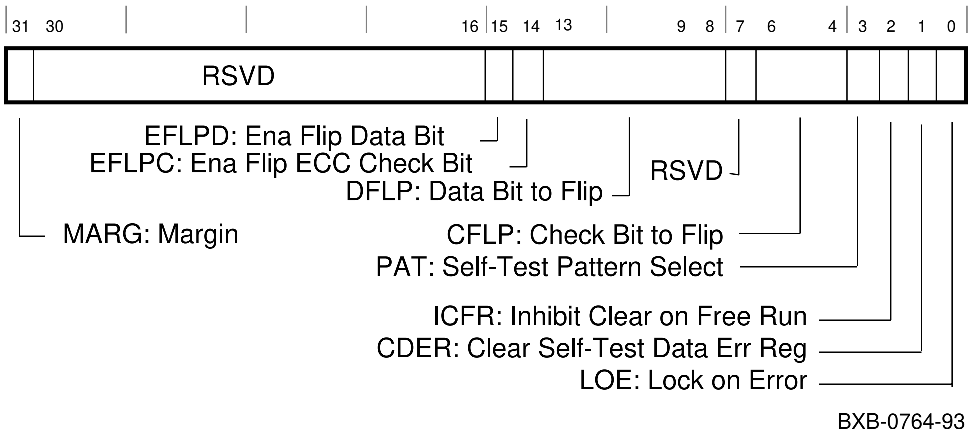


Table 2-20 DDRn Register Bit Definitions

Name	Bit(s)	Type	Function
MARG	<31>	R/W, 0	**Margin.** When set, margins the module's 3.35 volt DC to DC converters over a +/– 5% range. Register / Voltage / Margin DDR2 / 3.5 / +5% DDR3 / 3.5 / –5%
RSVD	<30:16>	R0	**Reserved.** Read as zero.

Table 2-20 DDRn Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
EFLPD	<15>	R/W, 0	**Enable Flip Data Bit.** When set in conjunction with MDRA<AMEN>, the data bit selected in DFLP<13:8> is flipped during memory write transactions. This function allows diagnostics to check ECC error detection logic. *NOTE: Setting both EFLPD and EFLPC results in Uncorrectable ECC written into memory.*
EFLPC	<14>	R/W, 0	**Enable Flip ECC Check Bit.** When set in conjunction with MDRA<AMEN>, the check bit selected in CFLP<6:4> will be flipped during memory write transactions. This function allows diagnostics to check ECC error detection logic. *NOTE: Setting both EFLPD and EFLPC results in Uncorrectable ECC written into memory.*
DFLP	<13:8>	R/W, 0	**Data Bit to Flip.** This field contains a hexadecimal value of the data bit to flip within a quadword during a memory write transaction when bit <15> (EFLPD) of this register is set and MDRA<AMEN> is set.
RSVD	<7>	R0	**Reserved.** Reads as zero.
CFLP	<6:4>	R/W, 0	**Check Bit to Flip.** This field contains a hexadecimal value of the check bit to flip within a quadword during a memory write transaction when bit <14> (EFLPC) of this register is set and MDRA<AMEN> is set.
PAT	<3>	R/W, 0	**Self-Test Pattern Select.** When set, self-test executes a defined data pattern required for the "moving inversion" self-test mode of operation. This bit in each of the four DDR registers and MDRA<MMPS> must be set to execute this special test mode.

Table 2-20 DDRn Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
ICFR	<2>	R/W, 0	**Inhibit Clear on Free Run.** When set in conjunction with MDRA<FRUN>, the contents of the STDER registers accumulate errors detected by self-test. When ICFR is cleared, the contents of the STDER registers will be cleared when self-test reenters the start execution phase due to <FRUN> set. This bit is valid only when self-test is in free run mode. If set during other self-test modes, operation is Undefined.
CDER	<1>	W, 0	**Clear Self-Test Data Error Registers.** When set, clears the Self-Test Data Error Registers (STDERA:E). This bit is normally used in conjunction with MDRA<POEM>. When <POEM> is set and an error is detected, self-test will halt and lock the error bit(s) in the STDERx_n registers. This function is normally exercised after an error halt, prior to continuing self-test (through <POEMC>) when in pause on error mode. Failure to set this bit following a POEM halt results in the STDERx_n registers accumulating past and possible future data bit errors.
LOE	<0>	R/W, 0	**Lock on Error.** When set, the contents of the STDERn registers and the contents of the STER registers lock and save the failing data bit(s), failing string, and which MDI4(s) detected the error upon the first detection of an error during pause on error mode self-test operation. If this bit is set during other self-test modes, operation is Undefined.

Chapter 3

Self-Test

Each module implements a built-in self-test to test the DRAM array and initialize the DRAMs with good ECC. Self-test's objectives during system operation are to initialize the array into a known state and, by flagging bad segments of memory, reduce the amount of time necessary for the console to locate and map out bad areas of physical address space. Self-test is invoked during system power-up, when a TLSB reset occurs, or by writing to the appropriate CSRs.

3.1 Self-Test Versions

Two versions of self-test are supported. A normal self-test that runs upon power-up/reset and tests the module rapidly and completely with "pseudo-random" data and address patterns. The test ensures detection of failures *prior* to booting an operating system. In summary, pseudo-random self-test leaves memory in the following states depending upon whether errors were detected:

- No errors detected
  - Memory initializes all locations with proper ECC.
  - The STF bit(s) are cleared and the LED is lit.
- Errors detected
  - Location(s) in error are written to an all ones pattern with uncorrectable ECC errors in the check field bits.
  - Error isolation information is logged into specific error registers.
  - The STF bit(s) are cleared and the LED is lit.

The second version of self-test, which is selected through diagnostic CSR writes, uses the *moving inversion* algorithm to detect DRAM sensitivity problems. This test (normally run in manufacturing only) is used to isolate DRAM sensitivity failures by using a test pattern (floating zeros) known to detect this class of failures. It executes 50 times slower than normal self-test due to the massive number of patterns and iterations that must be performed on each memory location.

3.2 Self-Test Modes

Self-test can be executed in three modes selectable through the MDRA register and the DDRn registers:

- Normal
- Pause on error (POEM)
- Free run (FRUN)

In a system environment, normal mode, test address and data patterns are generated in a pseudo-random fashion accessing all of memory space using the same primitive polynomials. TLSB self-test logic is partitioned into five gate arrays and uses four 72-bit test pattern generators.

Within POEM and FRUN, address and data can be generated pseudo-randomly, or with a moving inversion algorithm. Self-test Data Error registers (STDERn) in the MDI4 chips are used together with the Self-Test Error Register (STER) in the CTL4 to isolate down to the failing data bit during POEM mode testing.

Unlike normal mode, which stops after testing the entire array and clears the execute self-test bit, POEM and FRUN automatically loop on self-test until the operator clears MDRA<EXST>. When this occurs, self-test continues until the current loop is complete.

3.3 Self-Test Error Reporting

Self-test uses three registers to report errors. Table 3-1 shows which registers function in each test mode.

Table 3-1 Self-Test Error Registers

Register	Normal	Test Mode Pause on Error	Free Run
STAIR	On[1]	On	On
STER	Off[2]	On	Off
STDER	On	On	On

[1] The register is on during this mode of operation and must be verified for proper operation.

[2] No activity during this mode of operation.

During normal mode, errors are logged by flagging the segment of address space that contains the error. Any segment of memory that has one or more bad locations is indicated as such in the STAIR register. Errors are accumulated in the STDER register simply as a convenience.

During POEM mode, the STER and STDER registers are used to capture the failing string, MDI4 chip, and data bit(s) to isolate down to the failing chip during any DRAM failure. Although not necessary for chip isolation, the STAIR register operates as in normal mode.

During FRUN mode, the errors are accumulated in the STDER register. The STAIR register operates as in normal mode.

NOTE: The STDER registers are useless during FRUN mode if the pseudo-random pattern is selected. This is because if an error is detected in pass one of testing, an incorrect data pattern is intentionally written back to that location, *which causes all bits to fail in pass two. Therefore, all STDER registers in that MDI will be saturated.*

3.4 Self-Test Operation

Self-test is initiated whenever MDR<EXST> is set or a TLSB reset occurs. The DRAM state machine ignores requests for access to array space from the TLSB for the duration of testing. However, I/O registers may be accessed.

Self-test clears <EXST> upon completion. It also clears MCR<STF> upon successful completion.

NOTE: *Successful execution is not a measure of the array integrity. It indicates that every location in memory space has been tested and written with good or bad ECC.*

If node reset occurs during self-test, the array will be left in an unknown state. Unlike TLSB reset, node reset does not initiate self-test.

3.5 Self-Test Performance

The memory module's test time depends on the following parameters:

- DRAM size
- DRAM speed
- Memory array capacity
- Memory array architecture
- Clock speed

The self-test time is determined largely by the memory module's capacity. Tables 3-2 and 3-3 list the expected self-test times of various memory capacities based on a 10 ns bus clock. Test times during system power-up or TLSB reset are directly proportional to bus clock speed, because the optimum DRAM timing rate has not been loaded into the configuration register yet. Therefore, modules installed in a system with a 15 ns clock would take approximately 50 percent longer to test. If self-test is invoked with CSR commands after the console has selected the timing rate, test times should match the values given in Table 3-2 regardless of bus speed.

Table 3-2 Self-Test Times: Normal Mode

Module Capacity (Mbytes)	Test Time (seconds) 4-Mbit DRAM	16-Mbit DRAM	64-Mbit DRAM
128	.8	N/A[1]	N/A
256	1.5	1.5	N/A
512	2.9	2.9	N/A
1024	N/A	5.8	N/A
2048	N/A	11.5	N/A
4096	N/A	N/A	23.0

[1] NA = Not applicable

Table 3-3 Self-Test Times: Moving Inversion, No Errors Found

Module Capacity (Mbytes)	Test Time (minutes) 4-Mbit DRAM	16-Mbit DRAM	64-Mbit DRAM
128	.7	N/A[1]	N/A
256	1.4	1.4	N/A
512	2.7	2.7	N/A
1024	N/A	5.3	N/A
2048	N/A	10.6	N/A
4096	N/A	N/A	21.2

[1] NA = Not applicable

Index

X